CCS Technical Documentation
RH-3 Series Transceivers

Troubleshooting – BB

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Baseband Troubleshooting

RH-3 Baseband Module Overview

The Baseband module of the RH-3 transceiver is a CDMA dual-band engine. The baseband architecture is based on the other CDMA DCT4 phones, including NHP-2 and NPD-1, with a few modifications to support the RH-3 specific features (the new Pathfinder RF and GPS, which is reused from the NPD-4 program).

RH-3 cellular baseband consists of three ASICs: Universal Energy Management (UEM), Universal Phone Processor (UPP), and FLASH 64Megabit. There is a fourth BB ASIC implementing the GPS receiver in the phone.

The baseband architecture supports a power-saving function called *sleep mode*. This sleep mode shuts off the VCTCXO, which is used as system clock source for both RF and baseband. During the sleep mode, the system runs from a 32 kHz crystal and all the RF regulators (VR1A, VR1B, VR2, ... VR7) are off. The sleep time is determined by network parameters. Sleep mode is entered when both the MCU and the DSP are in standby mode and the normal VCTCXO clock is switched off. The phone is waken up by a timer running from this 32 kHz clock supply. The period of the sleep/wake up cycle (slotted cycle) is 1.28N seconds, where N= 0, 1, 2, depending on the slot cycle index.

RH-3 supports standard Nokia 2-wire and 3-wire chargers (ACP-x and LCH-x). However, the 3-wire chargers are treated as 2-wire chargers. The PWM control signal for controlling the three-wire charger is ignored. UEM ASIC and EM SW control charging.

BL-5C Li-ion battery is used as main power source for RH-3. BL-5C belongs to the new family of Lynx batteries. One of the biggest differences between the Lynx and the older batteries is that the temperature sensor for the battery has been removed from the batterypck and is placed in the phone. BL-5C has nominal capacity of 850 mAh.

RH-3 supports Tomahawk accessories. The system connector for the RH-3 phones is 14-pin Tomahawk connector. The accessories supported include headset (HDB-4), loopset (LPS-4), HF Basic Car Kit (BHF-1), advanced Car Kit (CarK-126), data cable (DKU-5), and the data/Flash cable (DKU-5F). The detection is based on the digital ID read from the accessories. For detail information, please refer *HDca2 BB module specification (DHX01477-EN).*

HW Architecture

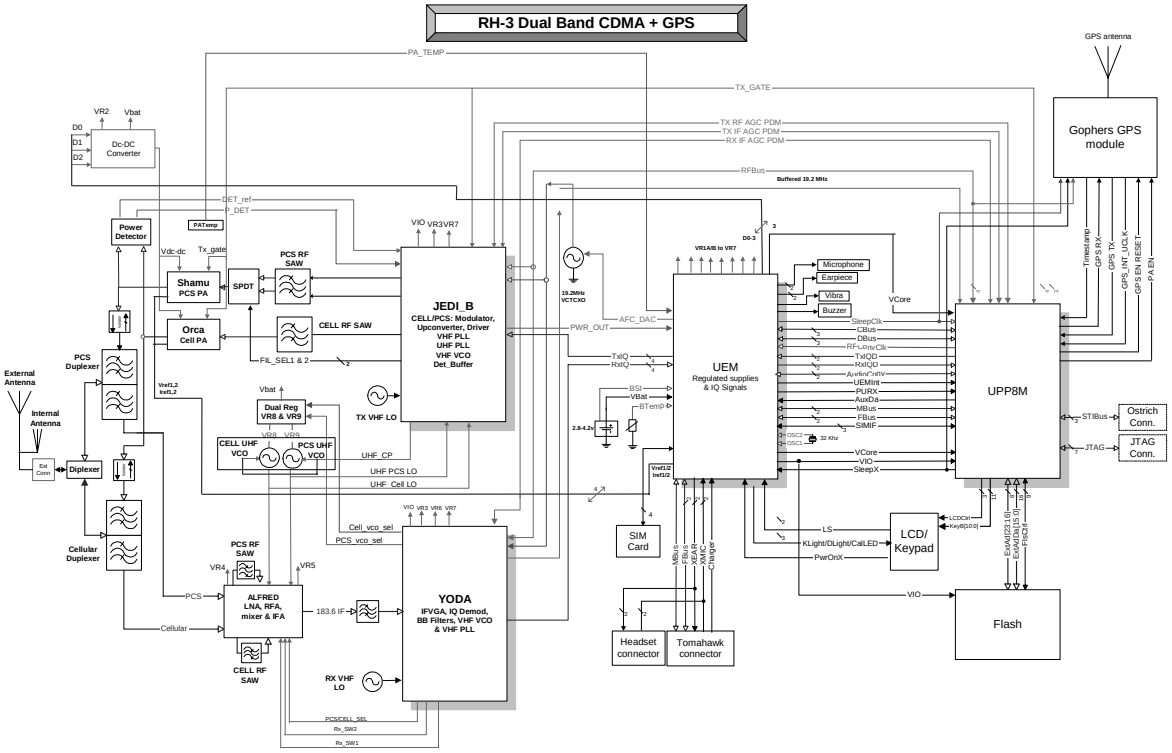

Figure 1: RH-3/RH-3P Top-level Diagram

Flash programming

Connections to Baseband

The Flash programming equipment is connected to the baseband using test pads for galvanic connection. The test pads are allocated in such a way that they can be accessed when the phone is assembled. The flash programming interface uses the VPP, FBUSTX, FBUSRX, MBUS, and BSI connections for the connection to the baseband. The connection is through the UEM, which means that the logic levels are corresponding to 2.7V. Power is supplied using the battery contacts.

Baseband Power Up

The baseband power is controlled by the flash prommer in production and in re-programming situations. Applying supply voltage to the battery terminals the baseband will power up. Once the baseband is powered, flash-programming indication is done as described in the following section.

Flash Programming Indication

Flash programming is indicated to the UPP using MBUSRX signal between UPP and UEM. The MBUS signal from the baseband to the flash prommer is used as clock for the synchronous communication. The flash prommer keeps the MBUS line low during UPP boot to indicate that the flash prommer is connected. If the UPP MBUSRX signal is low on UPP, the MCU enters flash programming mode. In order to avoid accidental entry to the flash-programming mode, the MCU only waits for a specified time to get input data from the flash prommer. If the timer expires without any data being received, the MCU will

continue the boot sequence. The MBUS signal from UEM to the external connection is used as clock during flash programming. This means that flash-programming clock is supplied to UPP on the MBUSRX signal.

The flash prommer indicates the UEM that flash programming/reprogramming by writing an 8-bit password to the UEM. The data is transmitted on the FBUSRX line and the UEM clocks the data on the FBUSRX line into a shift register. When the 8 bits have been shifted in the register, the flash prommer generates a falling edge on the BSI line. This loads the shift register content in the UEM into a compare register. If the 8 bits in the compare registers matches with the default value preset in the UEM, the flash prommer shall pull the MBUS signal to UEM low in order to indicate to the MCU that the flash prommer is connected. The UEM reset state machine performs a reset to the system, PURX low for 20 ms. The UEM flash programming mode is valid until MCU sets a bit in the UEM register that indicates the end of flash programming. Setting this bit also clears the compare register in the UEM previously loaded at the falling edge of the BSI signal. During the flash programming mode the UEM watchdogs are disabled. Setting the bit indicating end of flash programming enables and resets the UEM watchdog timer to its default value. Clearing the flash programming bit also causes the UEM to generate a reset to the UPP.

The BSI signal is used to load the value into the compare register. In order to avoid spurious loading of the register, the BSI signal will be gated during UEM master reset and during power on when PURX is active. The BSI signal should not change state during normal operation unless the battery is extracted; in this case, the BSI signal will be pulled high, note a falling edge is required to load the compare register.

Flashing

- Using FBUSTX, FBUSRX, MBUS, and BSI lines does flash programming.
- When phone is connected to the prommer, the prommer will first set BSI to "1" and then uses FBUSRX for writing and MBUS for clocking. The prommer will indicate to UEM that flash programming will take place by writing 8-bit password to UEM after BSI is set to high. After the password is checked, BSI is set back to "0". See Figure 1 on page 6.
- MCU will indicate to prommer that it has been noticed, by using FBUSTX signal. After this it reports UPP type ID and is ready to receive secondary boot code to its internal SRAM. (See Figure 2 on page 8).

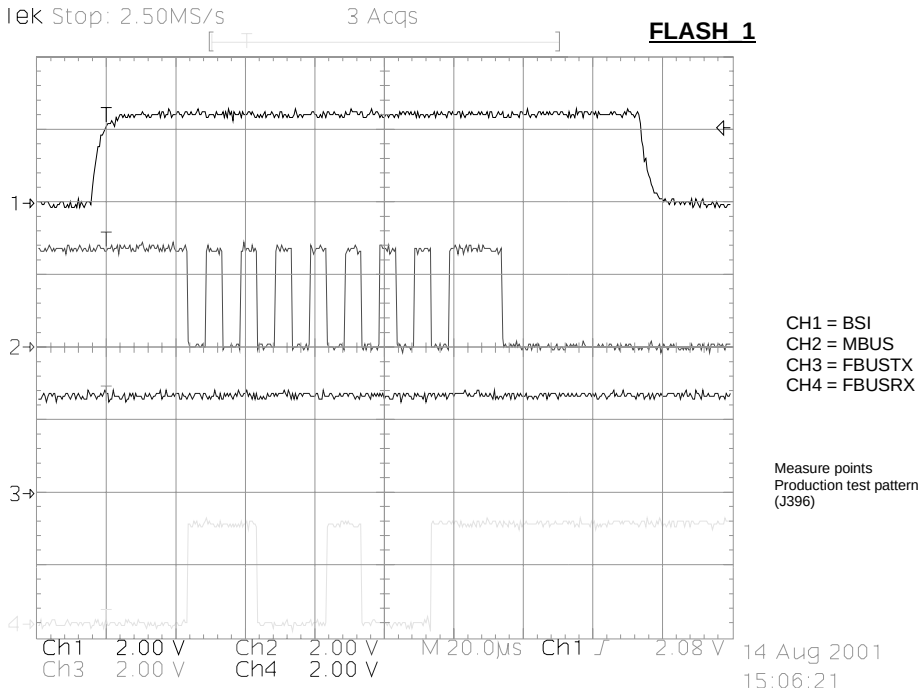

Figure 2: Flashing starts by BSI being pulled up and password being sent to UEM

- This boot code asks MCU to report prommer phone's configuration information, including flash device type. Now prommer can select and send algorithm code to MCU SRAM (and SRAM/Flash self-tests can be executed). (See Figure 3 on page 8 and Figure 4 on page 9.)

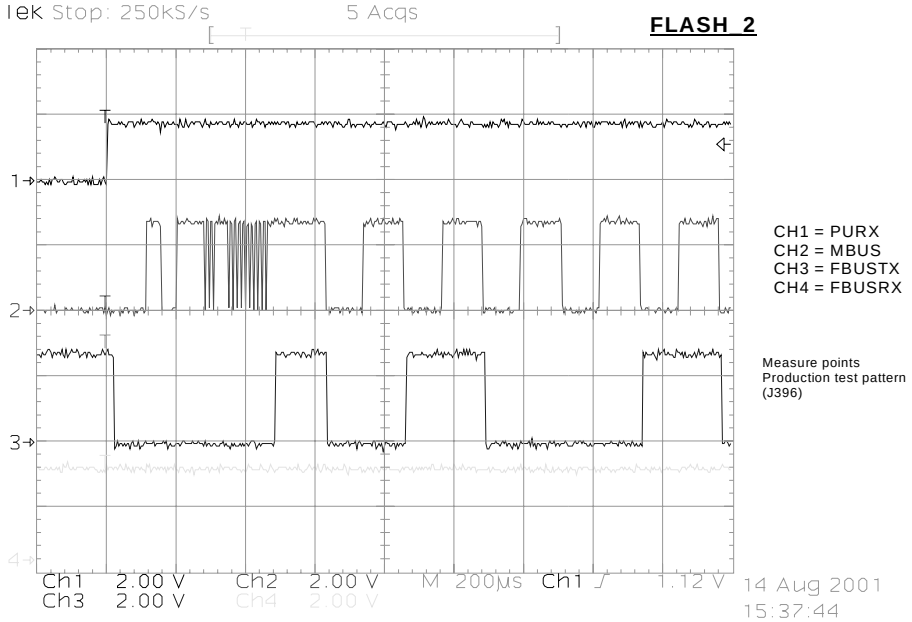

Figure 3: Flashing, continued

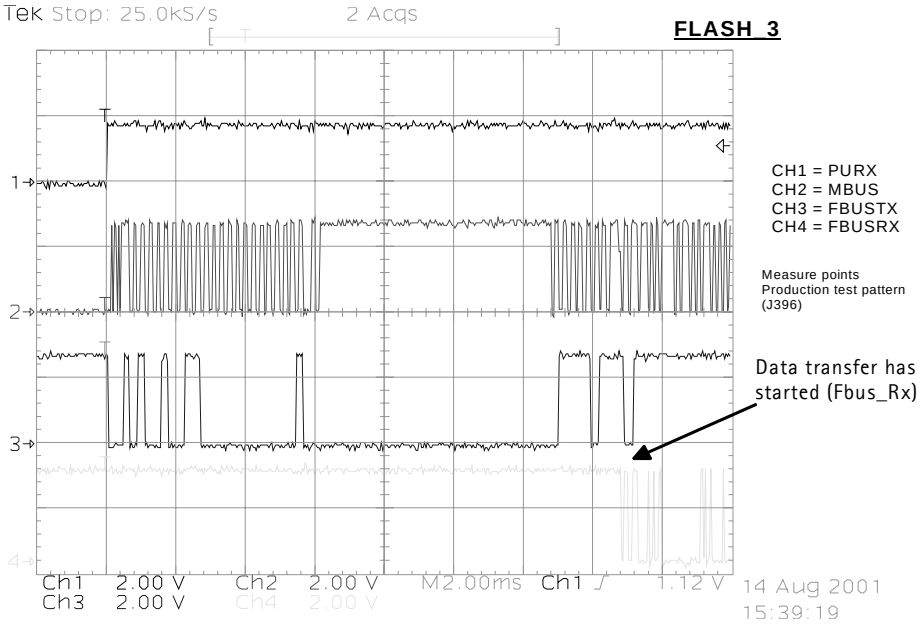

Figure 4: Flashing, continued

Power Up and Reset

Power up and reset is controlled by the UEM ASIC. RH-3 baseband can be powered up in the following ways:

- By the Power button, which means grounding the PWRONX pin of the UEM
- By connect the charger to the charger input
- By the RTC Alarm, when the RTC logic has been programmed to give an alarm

After receiving one of the above signals, the UEM counts a 20ms delay and then enters its reset mode. The watchdog starts up, and if the battery voltage is greater than Vcoff+, a 200ms delay is started to allow references, etc. to settle. After this delay elapses, the VFLASH1 regulator is enabled. Then, 500us later VR3, VANA, VIO, and VCORE are enabled. Finally the Power Up Reset (PURX) line is held low for 20 ms. This reset, PURX, is sent to UPP; resets are generated for the MCU and the DSP. During this reset phase, the UEM forces the VCTCXO regulator on — regardless of the status of the sleep control input signal to the UEM. The FLSRSTx from the UPP is used to reset the flash during power up and to put the flash in power down during sleep. All baseband regulators are switched on at the UEM power on — except for the SIM regulator and Vflash2. Vsim and Vflash2 are not used. The UEM internal watchdogs are running during the UEM reset state, with the longest watchdog time selected. If the watchdog expires, the UEM returns to power off state. The UEM watchdogs are internally acknowledged at the rising edge of the PURX signal in order to always give the same watchdog response time to the MCU.

The following timing diagram (Figure 5 on page 10) represents UEM start-up sequence

from reset to power-on mode.

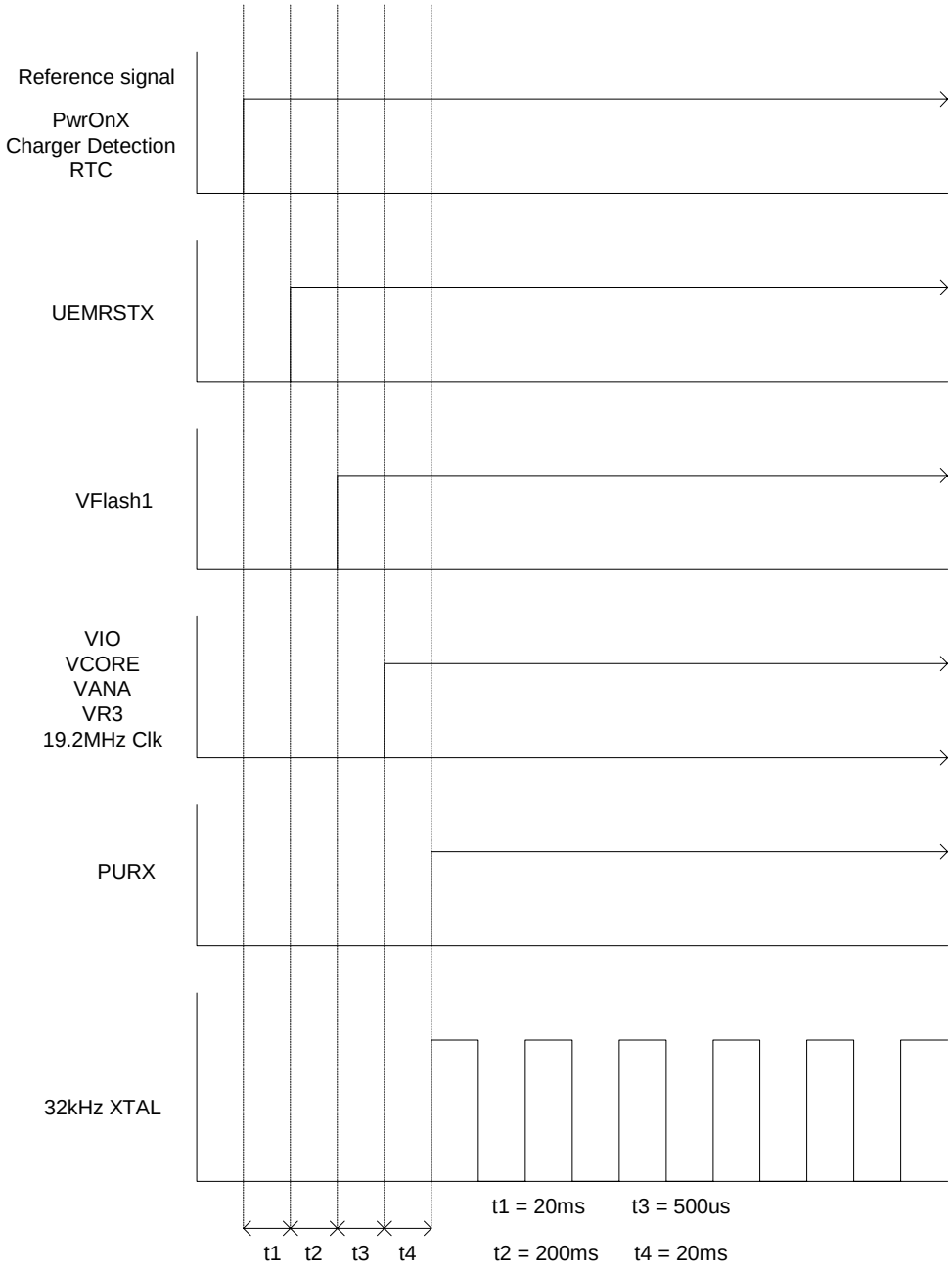

Figure 5: Power on sequence and timing

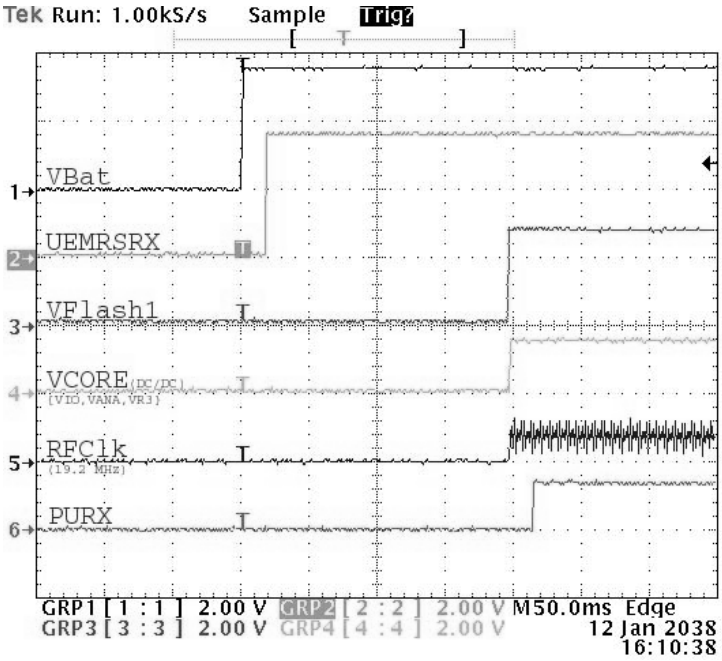
Tek Run: 1.00kS/s Sample Trig?
VBat
UEMRSRX
VFlash1
VCORE
RFClk
PURX
GRP1 [1 : 1] 2.00 V GRP2 [2 : 2] 2.00 V M50.0ms Edge
GRP3 [3 : 3] 2.00 V GRP4 [4 : 4] 2.00 V
12 Jan 2038
16:10:38

Figure 6: Measured power on sequence and timing

Power up with PWR key

When the Power on key is pressed, the UEM enters the power-up sequence. Pressing the power key causes the PWRONX pin on the UEM to be grounded. The UEM PWRONX signal is not part of the keypad matrix. The power key is only connected to the UEM. This means that when pressing the power key an interrupt is generated to the UPP that starts the MCU. The MCU then reads the UEM interrupt register and notice that it is a PWRONX interrupt. The MCU now reads the status of the PWRONX signal using the UEM control bus, CBUS. If the PWRONX signal stays low for a certain time the MCU accepts this as a valid power on state and continues with the SW initialization of the baseband. If the power on key does not indicate a valid power-on situation, the MCU powers off the baseband.

Power up when charger is connected

In order to be able to detect and start charging in a cases where the main battery is fully discharged (empty) and hence UEM has no supply (NO_SUPPLY or BACKUP mode of UEM), charging is controlled by *START-UP CHARGING* circuitry.

Whenever VBAT level is detected to be below master reset threshold (V_{MSTR-}), charging is controlled by START_UP charge circuitry. Connecting a charger forces VCHAR input to rise above charger detection threshold, VCH_{DET+}. By detection start-up charging is started. UEM generates 100mA constant output current from the connected charger's output voltage. As battery charges its voltage rises, and when VBAT voltage level higher than master reset threshold limit (V_{MSTR+}) is detected START_UP charge is terminated.

Monitoring the VBAT voltage level is done by charge control block (CHACON). MSTRX='1' output reset signal (internal to UEM) is given to UEM's *RESET* block when VBAT>V_{MSTR+}

and UEM enters into reset sequence.

If VBAT is detected to fall below V_{MSTR} during start-up charging, charging is cancelled. It will restart if new rising edge on VCHAR input is detected (VCHAR rising above VCH_{DET+}).

RTC alarm power up

If phone is in POWER_OFF mode when RTC alarm occurs the wake-up procedure. After baseband is powered on, an interrupt is given to MCU. When RTC alarm occurs during ACTIVE mode, the interrupt for MCU is generated.

Power off

The Baseband switch power-off mode if any of following statements is true:

- Power key is pressed
- Battery voltage is too low (VBATT < 3.2 V)
- Watchdog timer register expires

The Power-down procedure is controlled by the UEM.

Power Consumption and Operation modes

In the POWER-OFF mode, the power (VBAT) is supplied to UEM, VIBRA, LED-Driver, PA and PMIC.

In the SLEEP mode, both processors, MCU and DSP, are in stand-by mode. Both processors control sleep mode. When SLEEPX signal is detected low by the UEM, the phone enters SLEEP mode. VIO and VFLASH1 regulators are put into low quiescent current mode, and VANA and VFLASH2 regulators are disabled. All RF regulators are disabled during SLEEP mode. When SLEEPX signal is detected high by the UEM, the phone enters ACTIVE mode and all functions are activated.

The sleep mode is exited either by the expiration of a sleep clock counter in the UEM or by some external interrupt, generated by a charger connection, key press, headset connection, etc.

In sleep mode, VCTCXO is shut down and 32 kHz sleep clock oscillator is used as reference clock for the baseband.

The average current consumption of the phone in sleep mode can vary depending mainly on SW; however, on average is about 9 mA.

In the ACTIVE mode, the phone is in normal operation, scanning for channels, listening to a base station, transmitting and processing information. There are several sub-states in the active mode depending on the phone present state of the phone such as: burst reception, burst transmission, if DSP is working, etc.

In active mode the RF regulators are controlled by SW writing into UEM's registers wanted settings: VR1A and VR1B can be enabled or disabled. VSIM can be enabled or disabled and its output voltage can be programmed to be 1.8V or 3.3V. VR2 and VR4 - VR7 can be enabled or disabled or forced into low quiescent current mode. VR3 is always enabled in active mode and disabled during Sleep mode and cannot be control by SW.

In the CHARGING mode, the charging can be performed in parallel with any other operating mode. A BSI resistor inside the battery pack indicates the battery type/size. The resistor value corresponds to a specific battery capacity. This capacity value is related to the battery technology.

The battery voltage, temperature, size, and charging current are measured by the UEM, and the charging software running in the UPP controls it.

The charging control circuitry (CHACON) inside the UEM controls the charging current delivered from the charger to the battery and phone. The battery voltage rise is limited by turning the UEM switch off, when the battery voltage has reached 4.2 V. Charging current is monitored by measuring the voltage drop across a 220 mOhm resistor.

Power Distribution

In normal operation, the baseband is powered from the phone's battery. The battery consists of one Lithium-Ion cell capacity of 850 mAh, and some safety and protection circuits to prevent harm to the battery.

The baseband contains components that control power distribution to whole phone excluding the power amplifier (PA), which have a continuous power rail direct from the battery. The battery feeds power directly to following parts of the system: UEM, RF Pas, Vibra, Buzzer, Samrtcover Interface, and LED Driver.

The heart of the power distribution to the phone is the power control block inside UEM. It includes all the voltage regulators and feeds the power to the whole system. UEM handles hardware functions of power up so that regulators are not powered and power up reset (PURX) are not released if battery voltage is less than 3 V.

HDCA2 Baseband is powered from five different UEM regulators (VANA, VIO, VFLASH1, and VFLASH2) and the core voltage, which provide nominal voltages and currents according to Table 1.

UEM supplies also voltages VR1A, VR1B, VR2, VR3, VR4, VR5, VR6, and VR7 for RF. See Table 2.

Table 1: RH-3 Baseband regulators

Regulator	Maximum current (mA)	Vout (V)	Notes
VCORE	300	1.5	Output voltage selectable 1.0V/1.3V/1.5V/1.8V Power up default 1.5V
VIO	150	1.8	Enabled always except during power-off mode
VFLASH1	70	2.78	Enabled always except during power-off mode
VFLASH2	40	2.78	Enabled only when the system is awake (Off during sleep and power off-modes)
VANA	80	2.78	
VSIM	25	3.0	Enabled only when SIM card is used

Table 2: RH-3 RF regulators

Regulator	Maximum current (mA)	Vout (V)	Notes
VR1A	10	4.75	Enabled when cell transmitter is on
VR1B	10	4.75	Enabled when the PCS transmitter is on
VR2	100	2.78	Enabled when the transmitter is on
VR3	20	2.78	Enabled when SleepX is high
VR4	50	2.78	Enabled when the receiver is on
VR5	50	2.78	Enabled when the receiver is on
VR6	50	2.78	Enabled when the transmitter is on
VR7	45	2.78	Enabled when the receiver is on

The charge pump that is used by VR1A and VR1B is constructed around UEM. The charge pump works with 1.2 MHz oscillator and gives a 4.75 V regulated output voltage to RF.

Clock Distribution

RFClk (19.2 MHz Analog)

The main clock signal for the baseband is generated from the voltage and temperature controlled crystal oscillator VCTCXO (G500). This 19.2 MHz sine wave clock signal is fed to RFCLK pin of UPP. (See Figure 7 on page 15 for the waveform.)

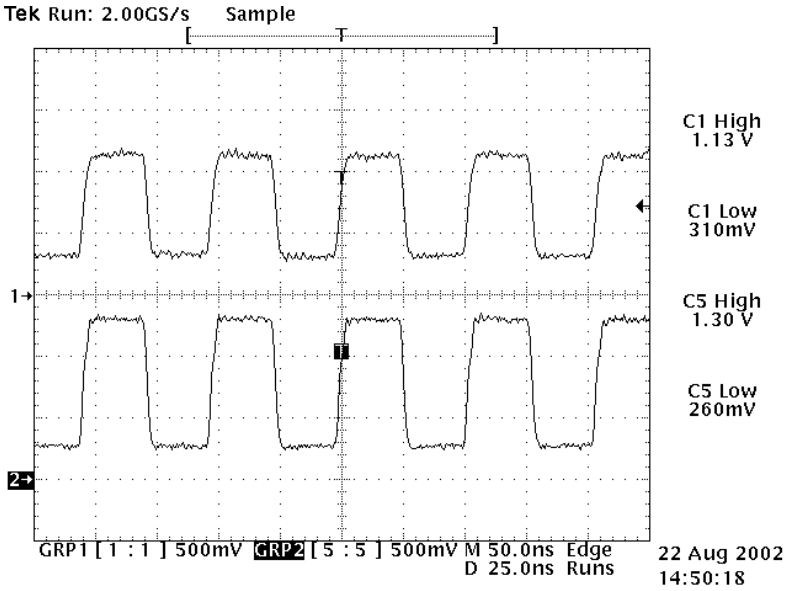

Figure 7: Waveform of 19.2MHz clock from RF to UPP and GPS BB Asic

RFConvClk (19.2 MHz digital)

The UPP distributes the 19.2MHz internal clock to the DSP and MCU, where SW multiplies this clock by seven for the DSP and by two for the MCU. (See Figure 8 on page 15.)

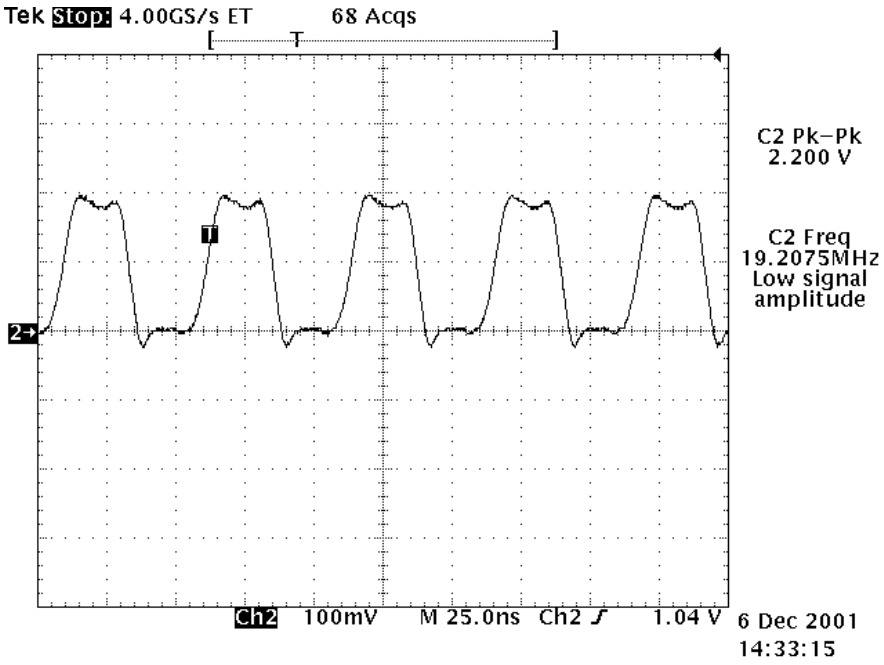

Figure 8: RFCovCLk waveform

CBUSClk Interface

A 1.2 MHz clock signal is use for CBUS, which is used by the MCU to transfer data between UEM and UPP. (See Figure 9 on page 16 for Cbus data transfer.)

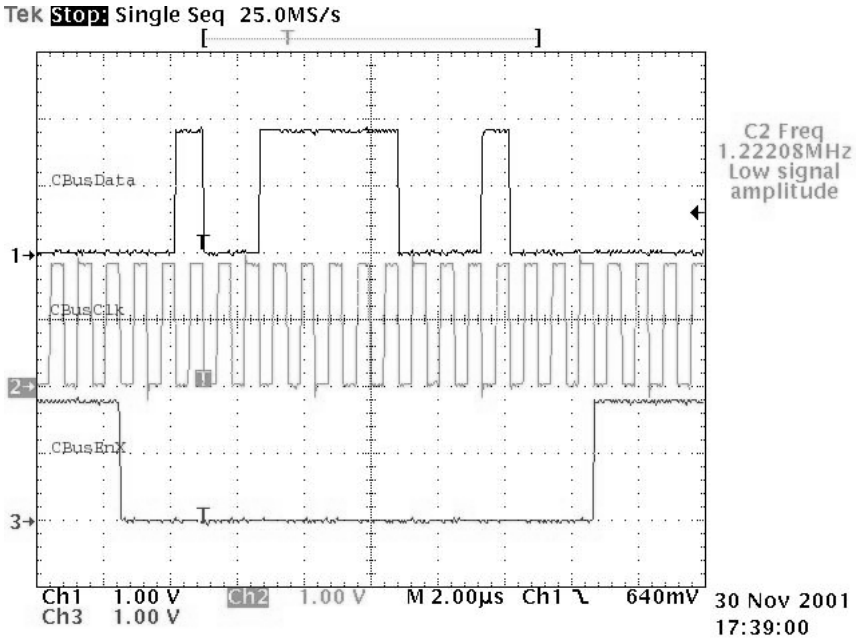

Figure 9: Cbus Data Transfer

DBUSClk Interface

A 9.6 MHz clock signal is use for DBUS, which is used by the DSP to transfer data between UEM and UPP. (See Figure 10 on page 16.)

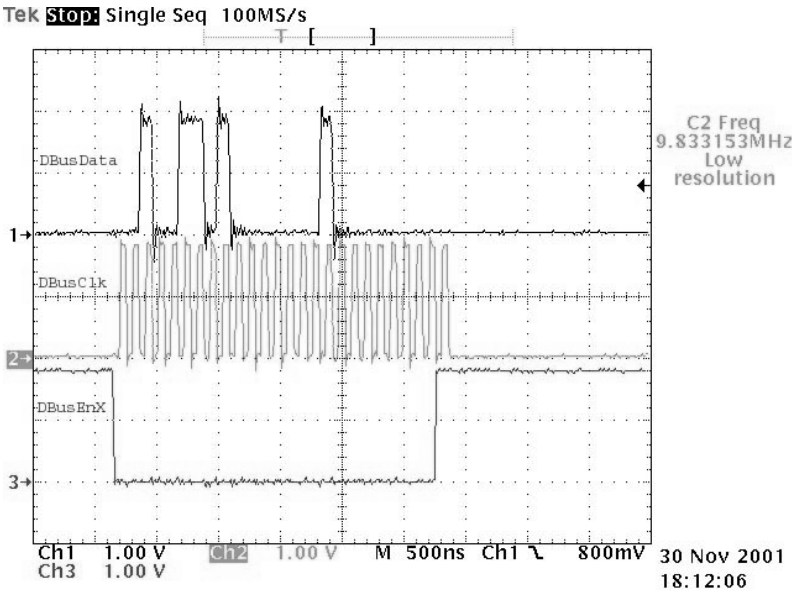

Figure 10: Dbus data transferring

The system clock is stopped during sleep mode by disabling the VCTCXO power supply (VR3) from the UEM regulator output by turning off the controlled output signal SleepX from UPP.

SLEEPClk (Digital)

The UEM provides a 32kHz sleep clock for internal use and to UPP, where it is used for the sleep mode timing. (Figure 11 on page 17.)

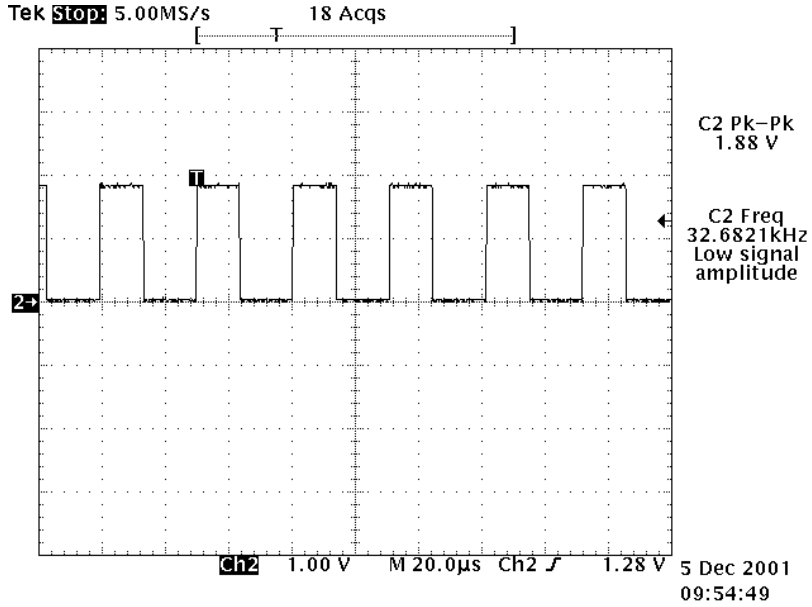

Figure 11: 32kHz Digital output from UEM

SLEEPClk (Analog)

However, when the system enters sleep mode or power off mode, the external 32KHz crystal provides a reference to the UEM RTC circuit to turn on the phone during porwer off or sleep mode. (See Figure 12 on page 17.)

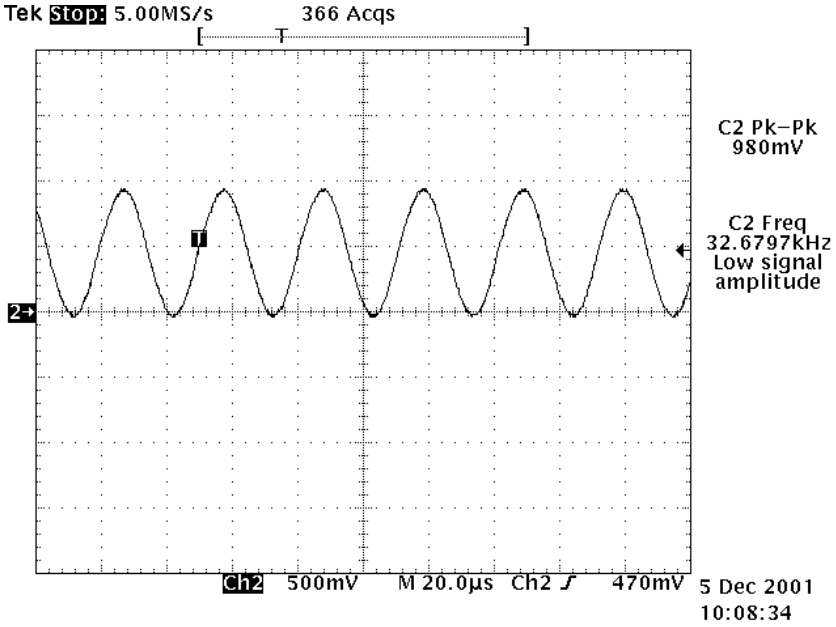

Figure 12: 32kHz analog waveform at 32KHz crystal input

Charging operation

Battery

In RH-3, a Lithium-Ion cell battery with a capacity of 850 mAh is used. Reading a resistor inside the battery pack on the BSI line indicates the battery type and size. The temperature sensor for BTEMP is inside the phone and position on the board in a way that it always has the same temperature as ther battery itself.

Temperature and capacity information are needed for charge control. The resistor for capacity info is connected to BSI pin of battery connector. Phone has 100 kΩ pull-up resistors for this line so that they can be read by A/D inputs in the phone.

See Figure 13 on page 18 and Figure 14 on page 18 for the details.

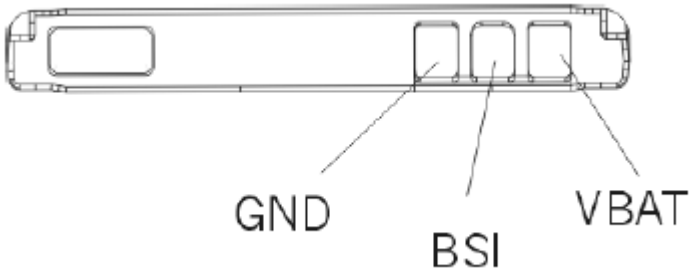

Figure 13: BL-5C battery pack pin order

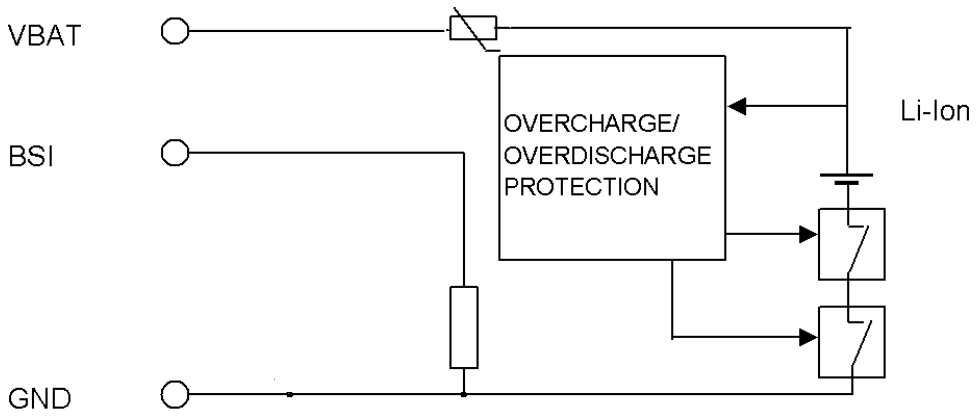

Figure 14: Interconnection diagram inside the battery pack

Charging circuitry

The UEM ASIC controls charging depending on the charger being used and the battery size. External components are needed for EMC, reverse polarity and transient protection of the input to the baseband module. The charger connection is through the system connector interface. The RH-3 baseband is designed to support DCT3 chargers from an electrical point of view. Both 2- and 3-wire type chargers are supported. For the 3-wire charger, the control line is not supported and not connected to the Baseband ASICs. See Figure 15 on page 19 for details.

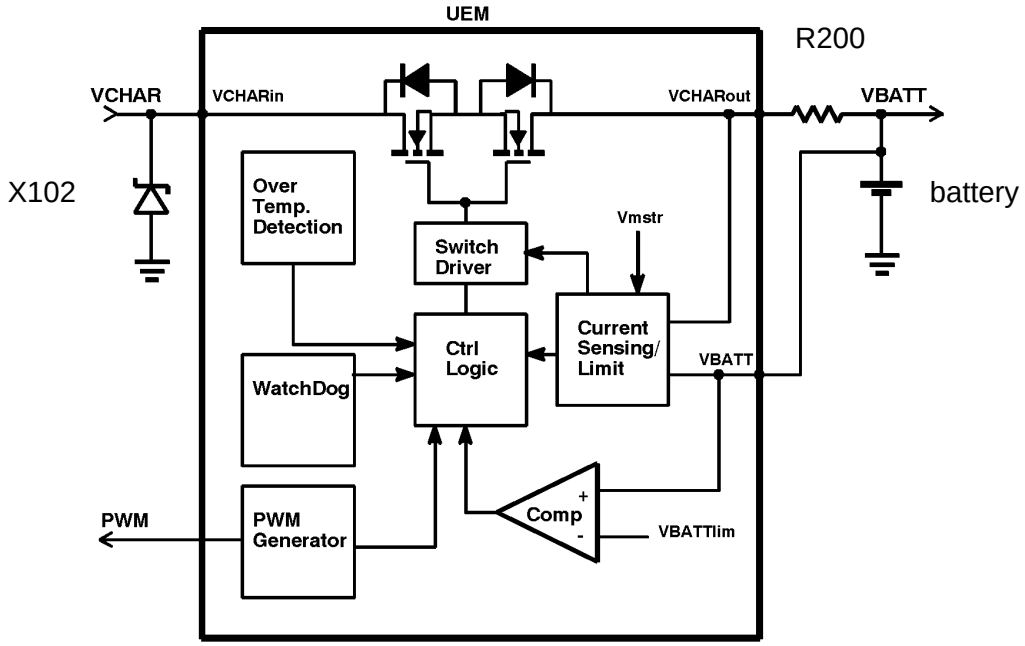

Figure 15: Charging circuitry

Charger Detection

Connecting a charger creates voltage on VCHAR input of the UEM. When VCHAR input voltage level is detected to rise above 2 V (VCHdet+ threshold) by UEM charging starts. VCHARDET signal is generated to indicate the presence of the charger for the SW. The charger identification/acceptance is controlled by EM SW.

The charger recognition is initiated when the EM SW receives a "charger connected" interrupt. The algorithm basically consists of the following three steps:

1 Check that the charger output (voltage and current) is within safety limits.

2 Identify the charger as a two-wire or three-wire charger.

3 Check that the charger is within the charger window (voltage and current).

If the charger is accepted and identified, the appropriate charging algorithm is initiated.

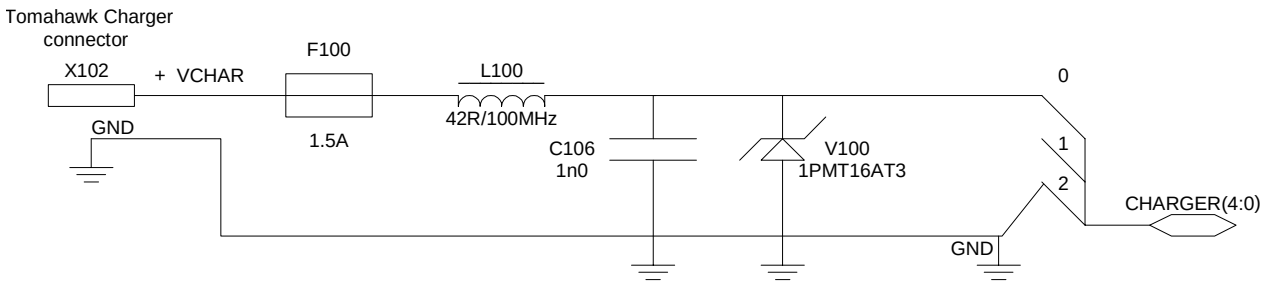

Figure 16: Charging circuit

Charge Control

In active mode charging is controlled by UEM's digital part. Charging voltage and current monitoring is used to limit charging into safe area. For that reason UEM has programmable charging cut-off limits:

VBATLim1=3.6 V (Default)

VBATLim2L=5.0 V and

VBATLim2H=5.25 V.

VBATLim1, 2L, 2H are designed with hystereses. When the voltage rises above VBATLim1, 2L, 2H+ charging is stopped by turning charging switch OFF. No change in operational mode is done. After voltage has decreased below VBATLim- charging re-starts.

There are two PWM frequencies in use depending on the type of the charger: two-wire charger uses a 1Hz and a three-wire charger uses a 32Hz. Duty cycle range is 0% to 100%. Maximum charging current is limited to 1.2 A.

Audio

The audio control and processing in RH-3 is provided by UEM, which contains the audio codec, and UPP — which contains the MCU and DSP blocks, handling and processing the audio data signals.

The baseband supports three microphone inputs and two earpiece outputs. The microphone inputs are MIC1, MIC2, and MIC3. MIC1 input is used for the phone's internal microphone; MIC2 input is used for headsets (HDB-4, BHF-1. and CarK-126), Loopset (LPS-4). MIC3 input is used for third-party accessories (2.5mm Jack). Every microphone input can have either a differential or single ended ac connection to UEM circuit. In RH-3, the internal microphone (MIC1) and MIC2 are differential and MIC3 microphones are single-ended. The microphone signals from different sources are connected to separate inputs at UEM. Inputs for the microphone signals are differential type. Also, MICBIAS1 is used for MIC1 and MICBIAS2 is used for MIC2 and MIC3.

Display and Keyboard

LEDs are used for LCD and keypad illumination in RH-3. There are three LEDs for LCD and four LEDs for keypad. The LEDs are supplied by a driver circuit which consists of a charge pump and several current source, which are partly integrated into the driver and partly realized by discretes.

A monochrome LCD is used in RH-3. Interface is using 9-bit data transfer. The interface is quite similar to DCT3 type interface, except Command/Data information is transferred together with the data. D/C bit set during each transmitted byte by MCU SW.

Figure 17 on page 21 is the waveform for LCD interface.

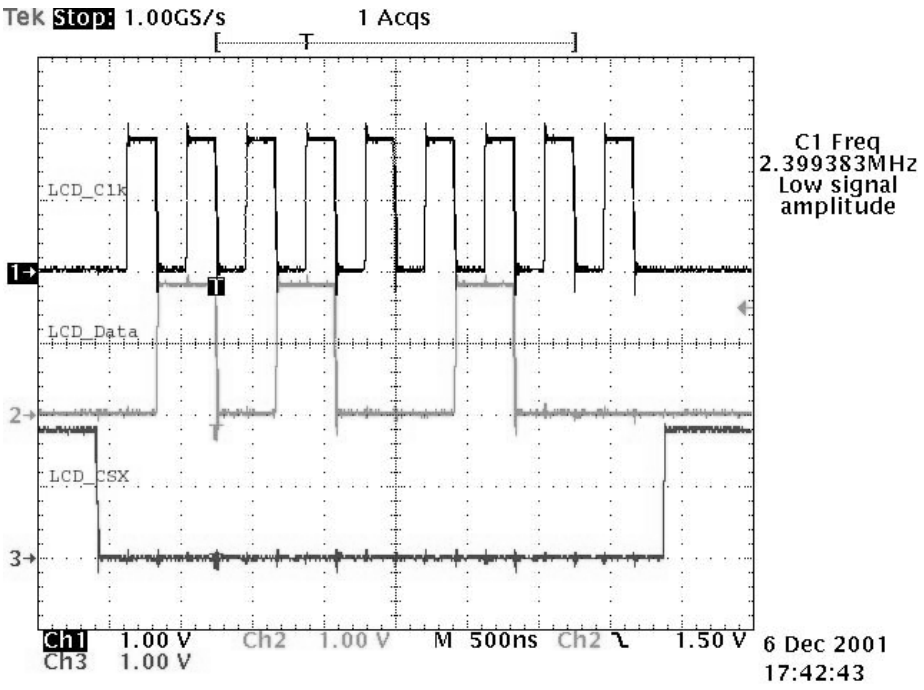

Figure 17: LCD Interface

Accessory

RH-3 is designed to support differential ended external audio accessory connection. Headset and data cables can be directly connected to system connector or 2.5mm jack supporting TTY/TDD or universal headset. Detection of the different accessories is based on the ACI code residing inside the accessories except for basic headset (HDB-4) and universal headset. The UHJ is detected by the interrupt generated on GenIO (12). The basic headset is detected via ACI detection algorithm. However, the ACI pin is always grounded.

It is end user's responsibility to set the phone for TTY/TDD since there are too many different TTY/TDD devices to be detected.

Test Points

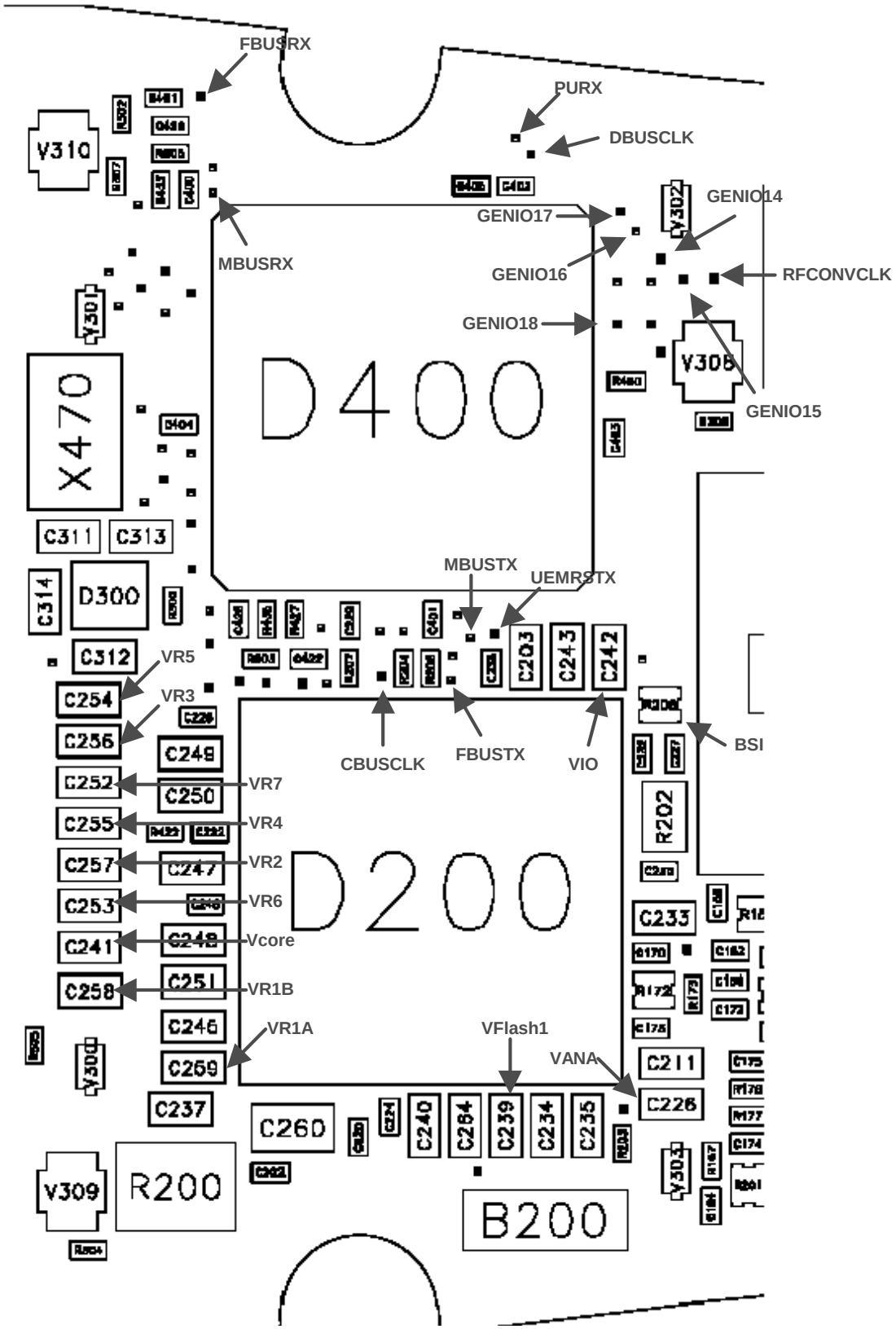

Figure 18: RH-3 BB test points, regulators, and BB ASICs

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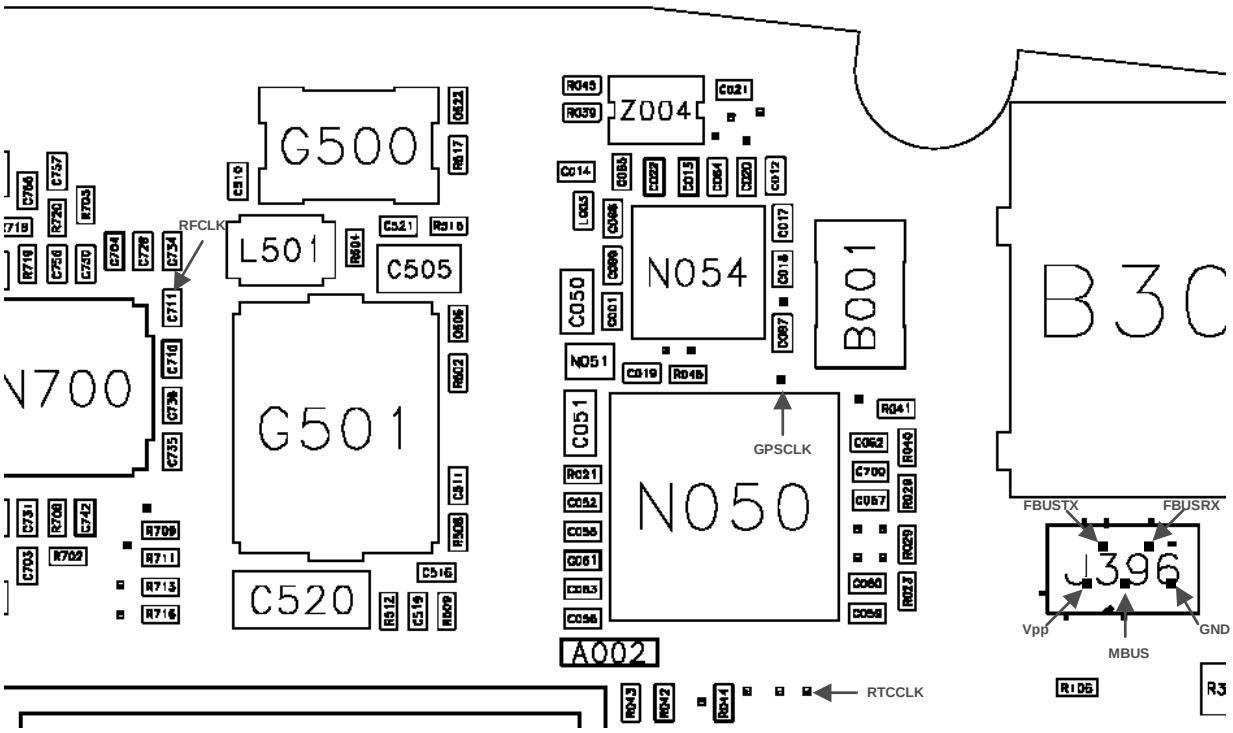


Figure 19: RH-3 BB test points, regulators, and BB ASICs

Troubleshooting

The following hints should help finding the cause of the problem when the circuitry seems to be faulty. Troubleshooting instructions are divided following sections:

1 Top troubleshooting map

2 Phone is totally dead

3 Power doesn't stay on or the phone is jammed

4 Flash programming doesn't work

5 Display is not working

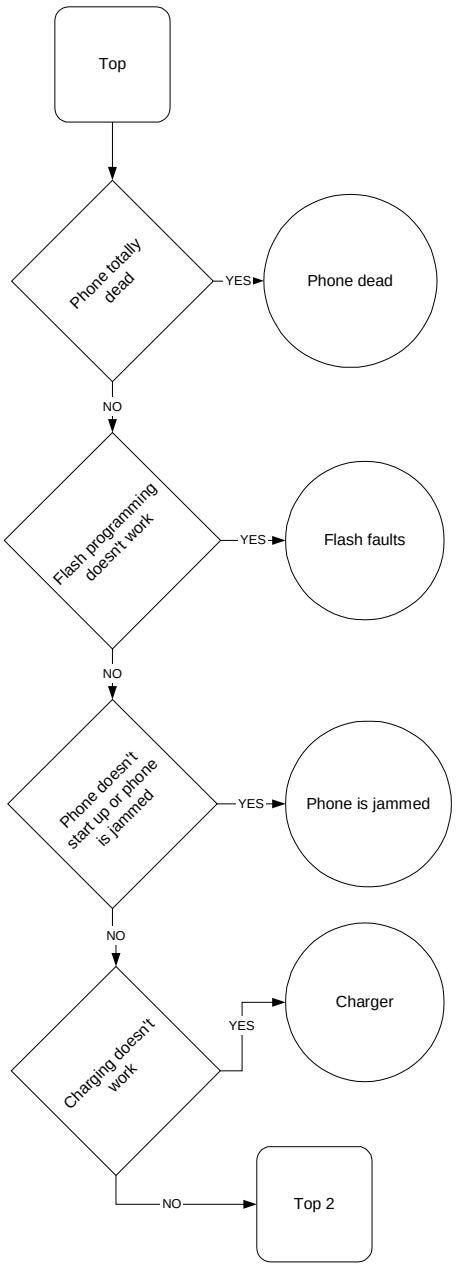
6 Audio fault

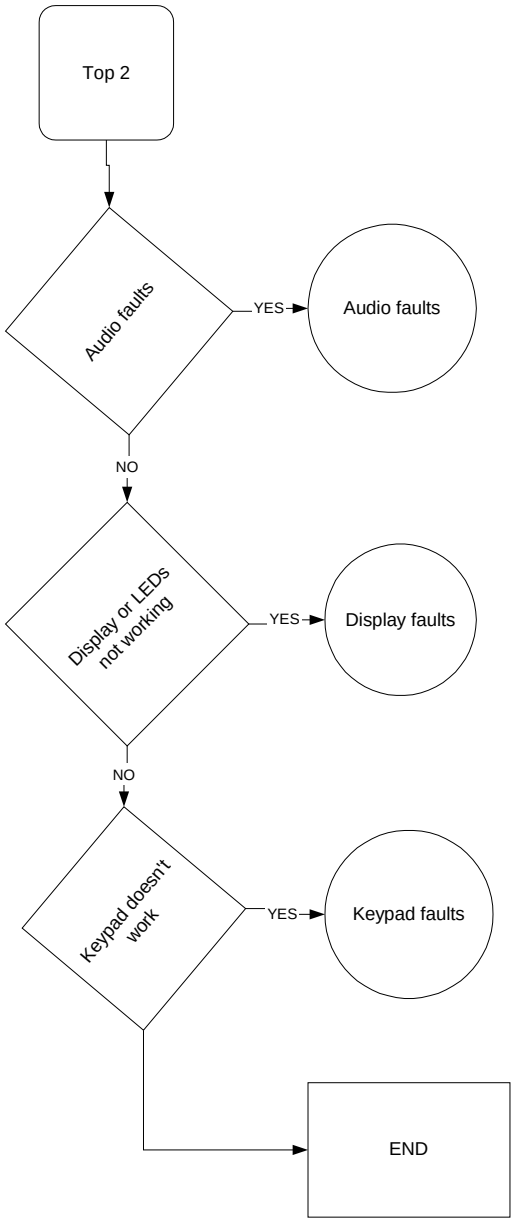
7 Charging fault

First, carry out a through visual check of the module. Ensure in particular that:

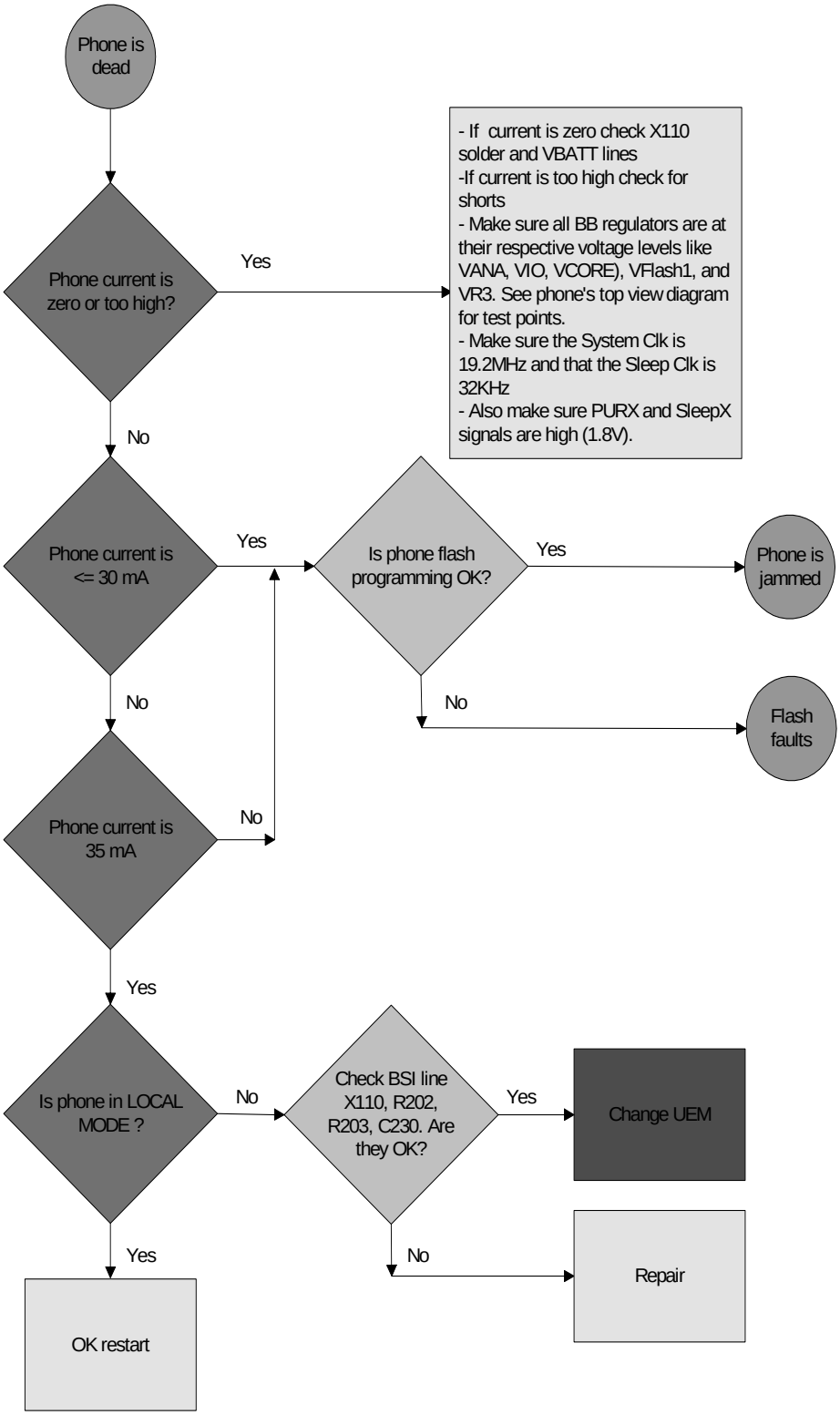
- there are no mechanical damages
- soldered joints are OK
- ASIC orientations are OK

Top troubleshooting map

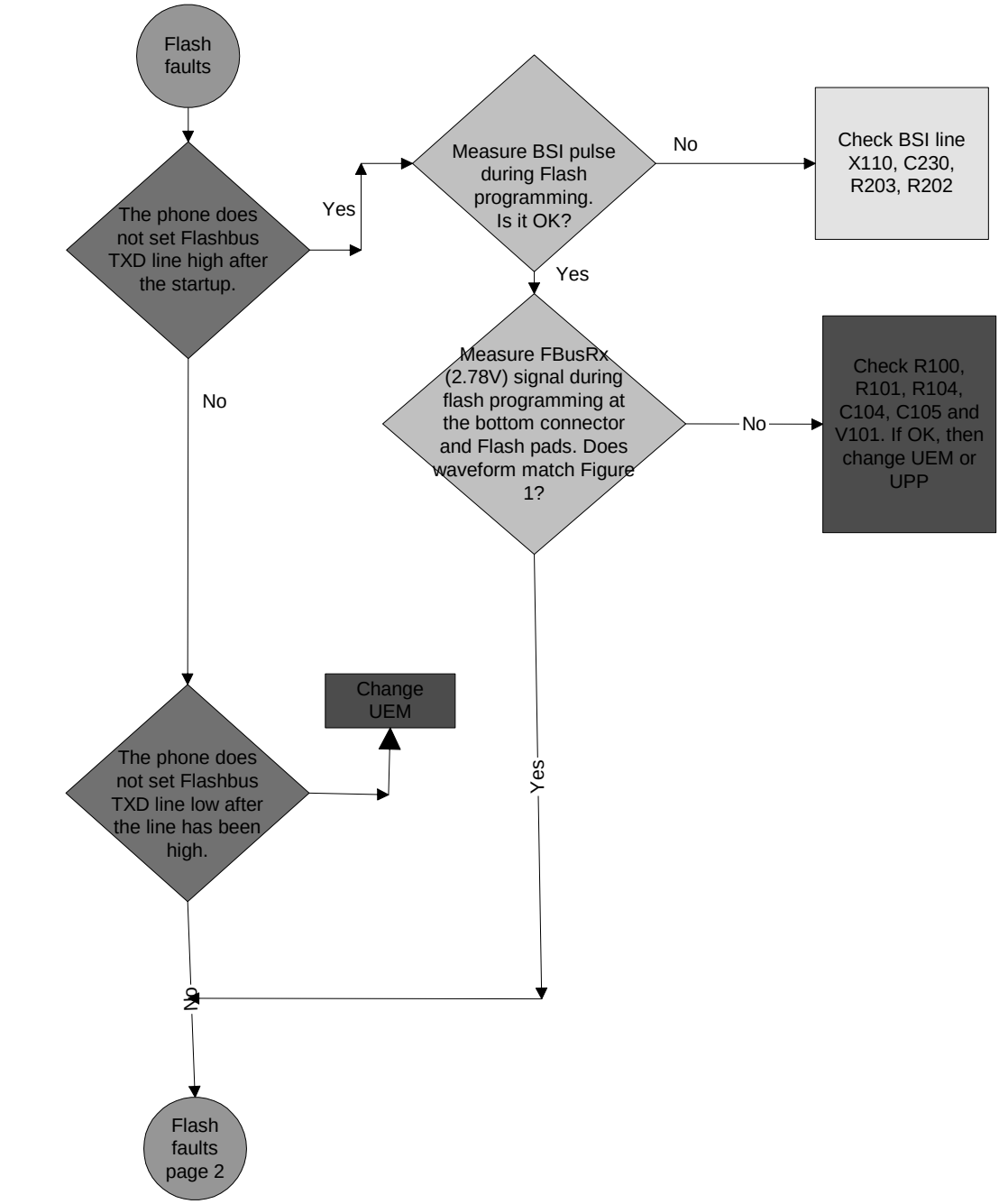


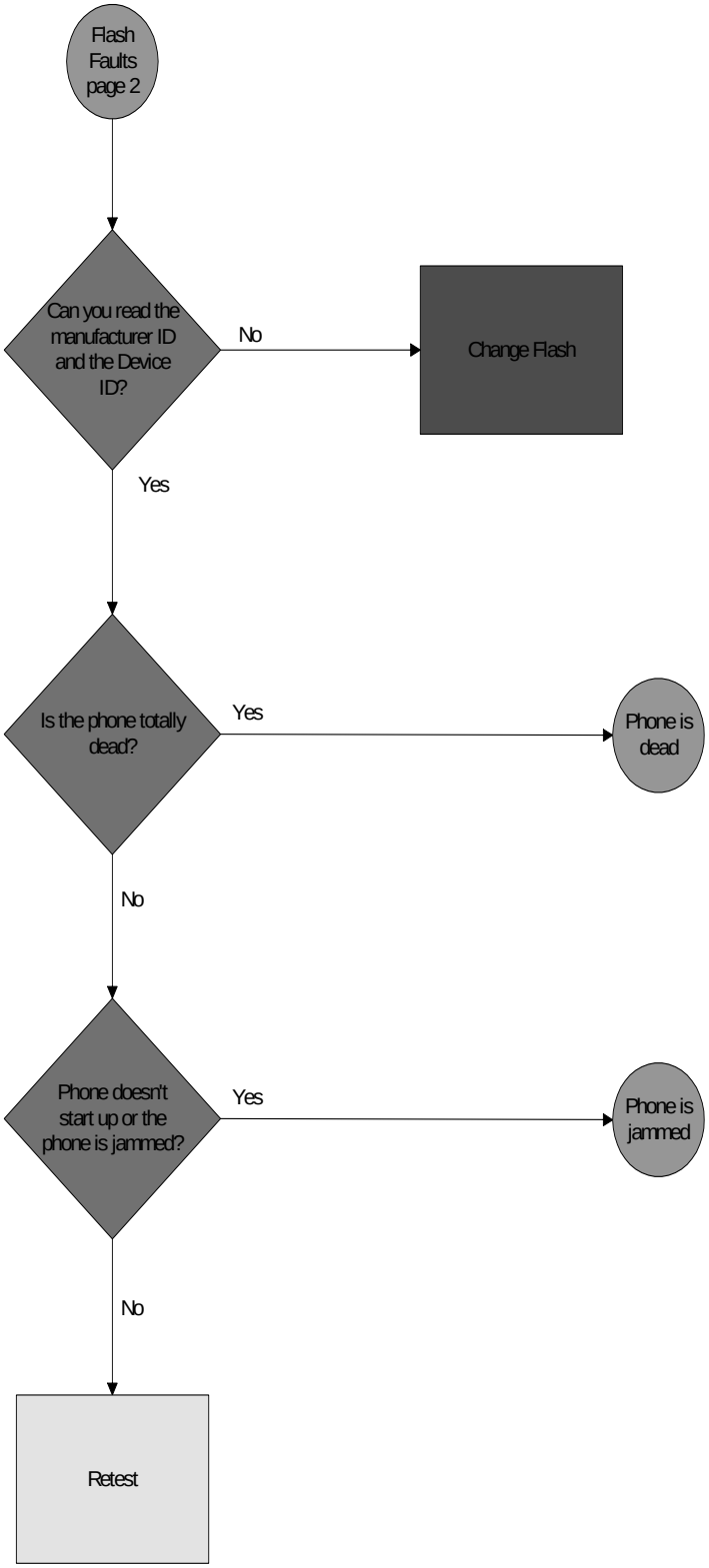

Top 2
Audio faults
YES
Audio faults
NO
Display or LEDs not working
YES
Display faults
NO
Keypad doesn't work
YES
Keypad faults
END

Phone is totally dead

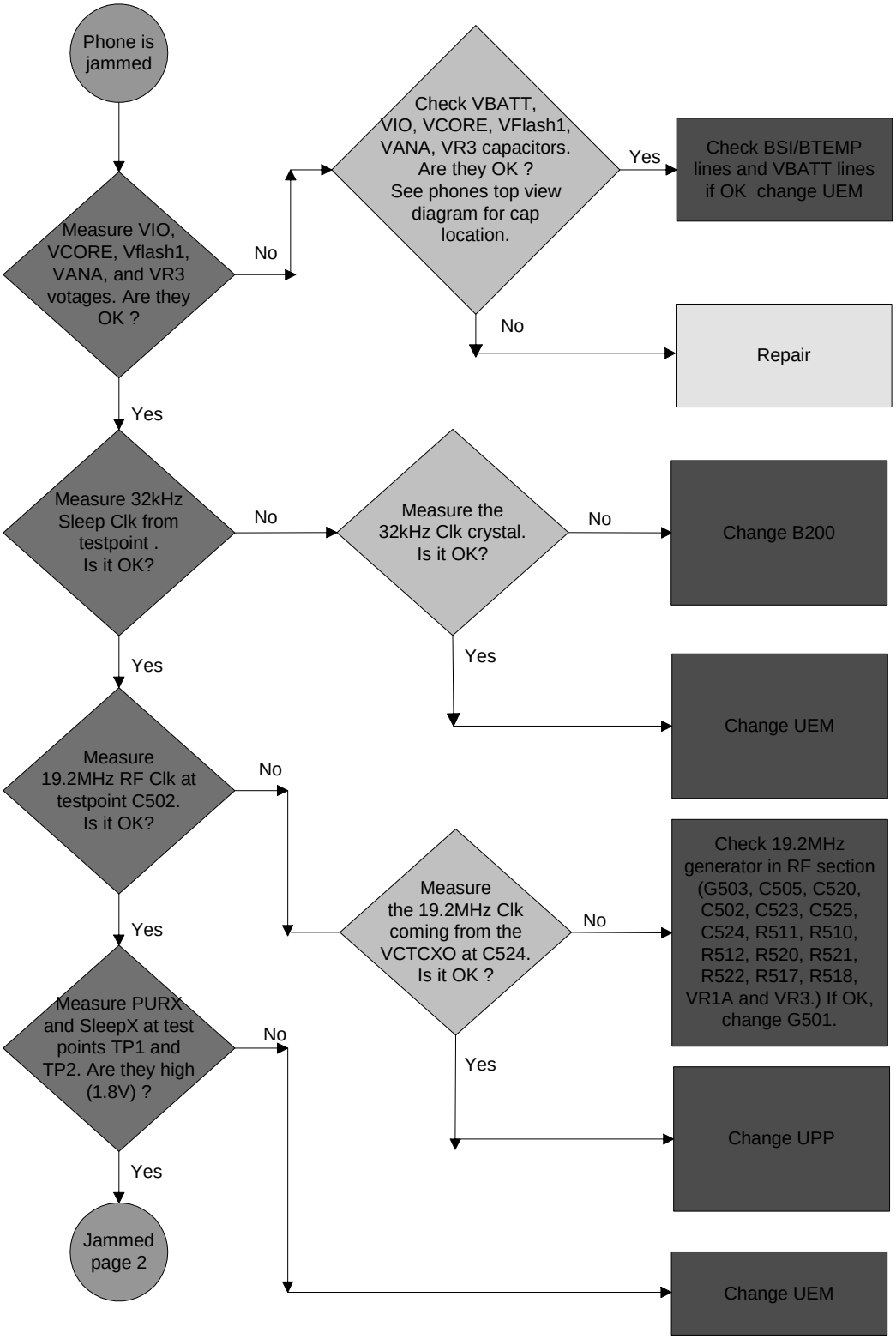

Phone is dead
Phone current is zero or too high?
Yes
- If current is zero check X110 solder and VBATT lines
-If current is too high check for shorts
- Make sure all BB regulators are at their respective voltage levels like VANA, VIO, VCORE), VFlash1, and VR3. See phone's top view diagram for test points.
- Make sure the System Clk is 19.2MHz and that the Sleep Clk is 32KHz
- Also make sure PURX and SleepX signals are high (1.8V).
No
Phone current is <= 30 mA
Yes
Is phone flash programming OK?
Yes
Phone is jammed
No
Flash faults
Phone current is 35 mA
No
Yes
Is phone in LOCAL MODE ?
No
Check BSI line X110, R202, R203, C230. Are they OK?
Yes
Change UEM
Yes
OK restart
No
Repair

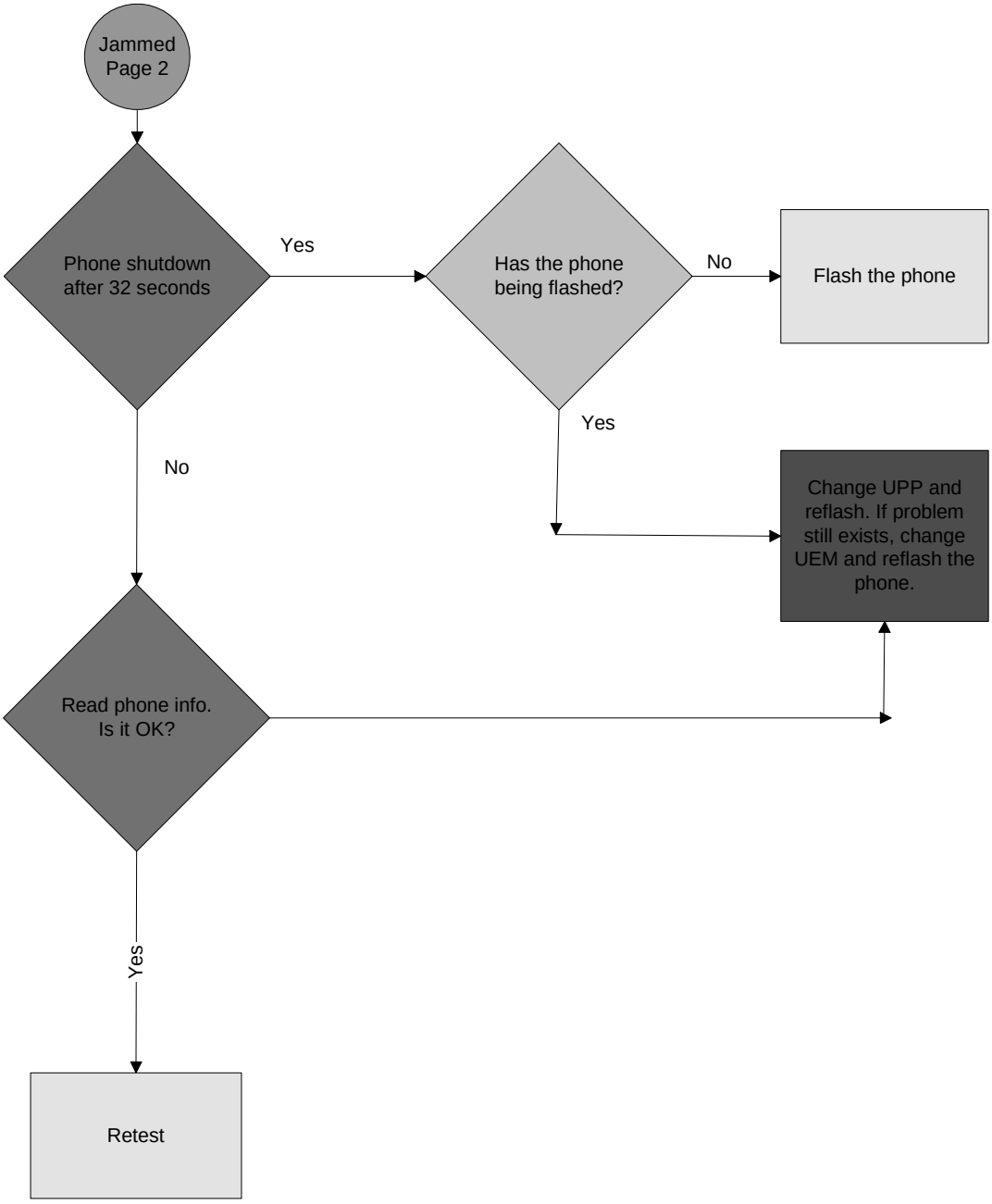
Flash programming doesn't work


Flash faults
The phone does not set Flashbus TXD line high after the startup.
Yes
Measure BSI pulse during Flash programming. Is it OK?
No
Check BSI line X110, C230, R203, R202
Yes
Measure FBusRx (2.78V) signal during flash programming at the bottom connector and Flash pads. Does waveform match Figure 1?
No
Check R100, R101, R104, C104, C105 and V101. If OK, then change UEM or UPP
No
Change UEM
The phone does not set Flashbus TXD line low after the line has been high.
Yes
No
Flash faults page 2

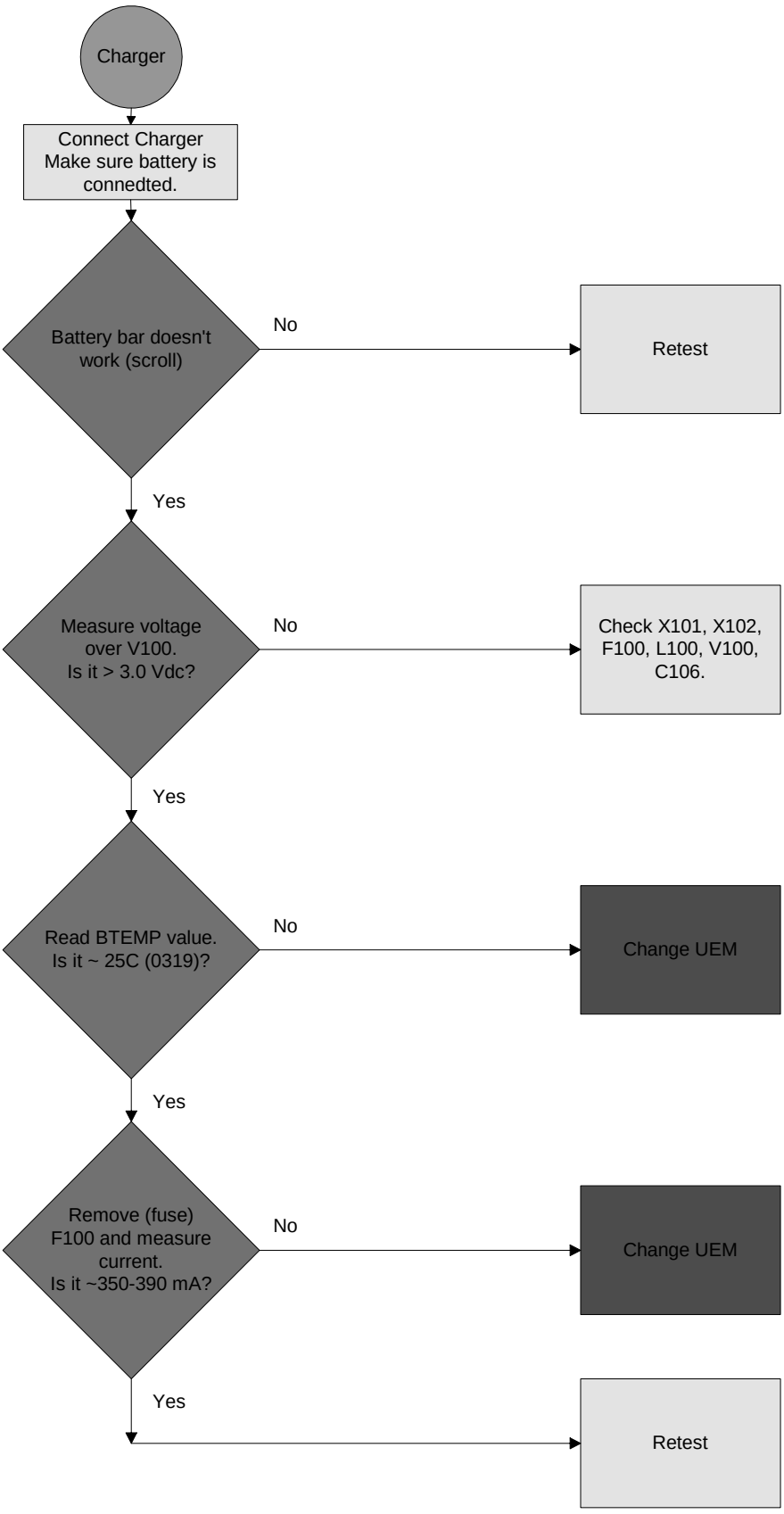

Flash Faults page 2
Can you read the manufacturer ID and the Device ID?
No
Change Flash
Yes
Is the phone totally dead?
Yes
Phone is dead
No
Phone doesn't start up or the phone is jammed?
Yes
Phone is jammed
No
Retest

Power doesn't stay on or the phone is jammed

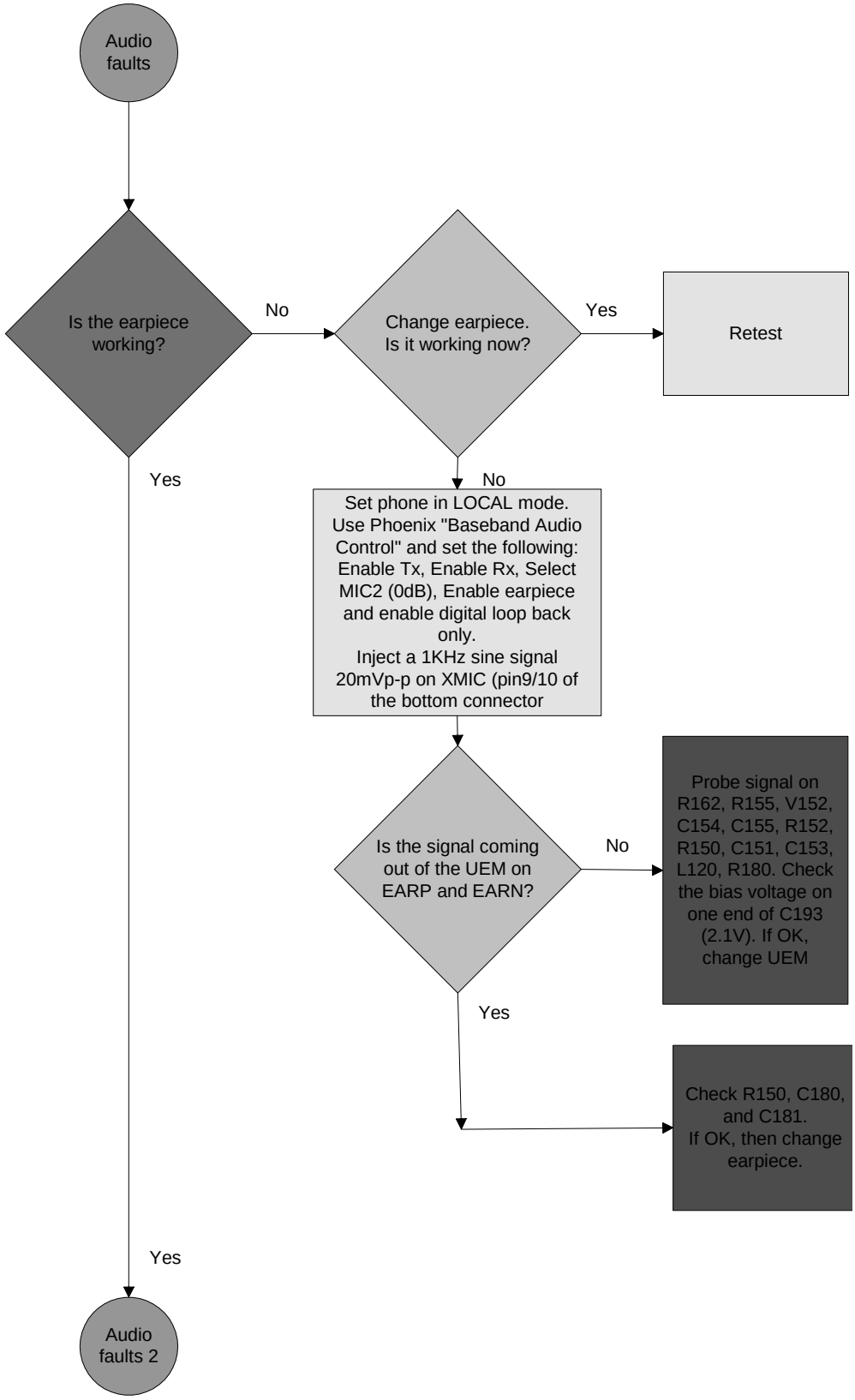

Phone is jammed
Measure VIO, VCORE, Vflash1, VANA, and VR3 votages. Are they OK ?
No
Check VBATT, VIO, VCORE, VFlash1, VANA, VR3 capacitors. Are they OK ? See phones top view diagram for cap location.
Yes
Check BSI/BTEMP lines and VBATT lines if OK change UEM
No
Repair
Yes
Measure 32kHz Sleep Clk from testpoint . Is it OK?
No
Measure the 32kHz Clk crystal. Is it OK?
No
Change B200
Yes
Change UEM
Yes
Measure 19.2MHz RF Clk at testpoint C502. Is it OK?
No
Measure the 19.2MHz Clk coming from the VCTCXO at C524. Is it OK ?
No
Check 19.2MHz generator in RF section (G503, C505, C520, C502, C523, C525, C524, R511, R510, R512, R520, R521, R522, R517, R518, VR1A and VR3.) If OK, change G501.
Yes
Measure PURX and SleepX at test points TP1 and TP2. Are they high (1.8V) ?
No
Yes
Change UPP
Yes
Jammed page 2
Change UEM

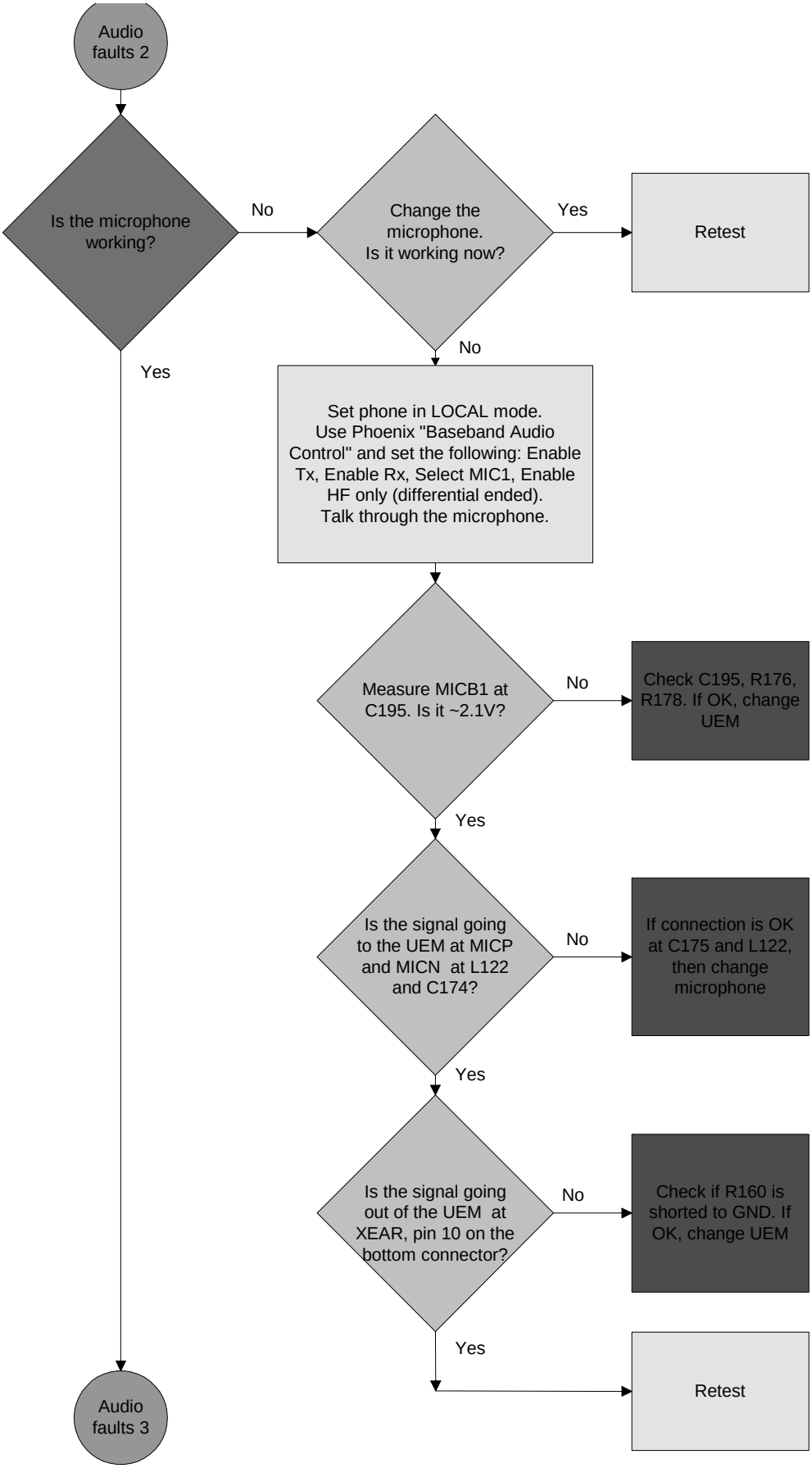

Jammed
Page 2
Phone shutdown
after 32 seconds
Yes
Has the phone
being flashed?
No
Flash the phone
Yes
No
Change UPP and
reflash. If problem
still exists, change
UEM and reflash the
phone.
Read phone info.
Is it OK?
Yes
Retest

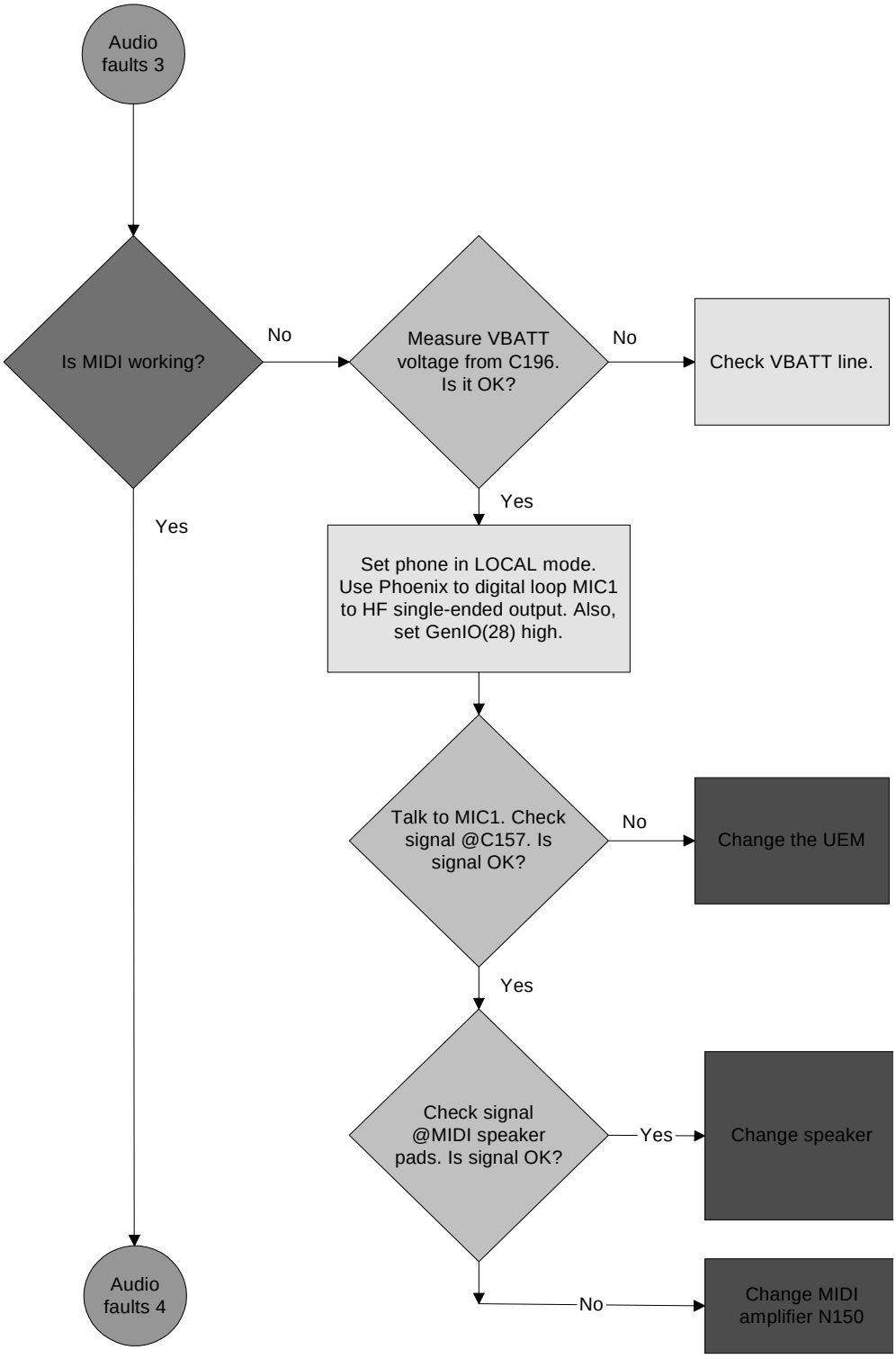
Charger

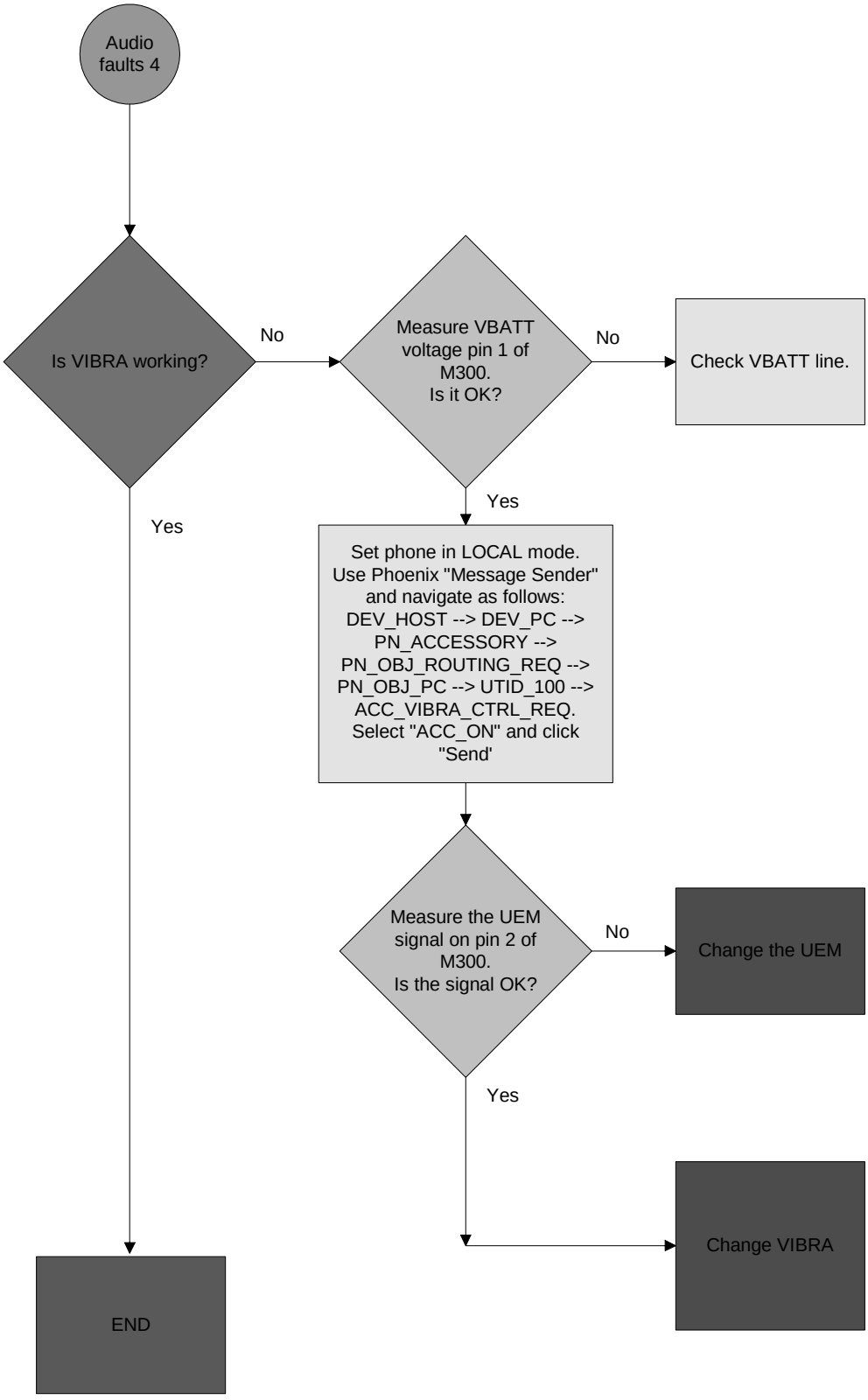

Charger
Connect Charger
Make sure battery is connedted.
Battery bar doesn't work (scroll)
No
Retest
Yes
Measure voltage over V100.
Is it > 3.0 Vdc?
No
Check X101, X102, F100, L100, V100, C106.
Yes
Read BTEMP value.
Is it ~ 25C (0319)?
No
Change UEM
Yes
Remove (fuse) F100 and measure current.
Is it ~350-390 mA?
No
Change UEM
Yes
Retest

Audio faults

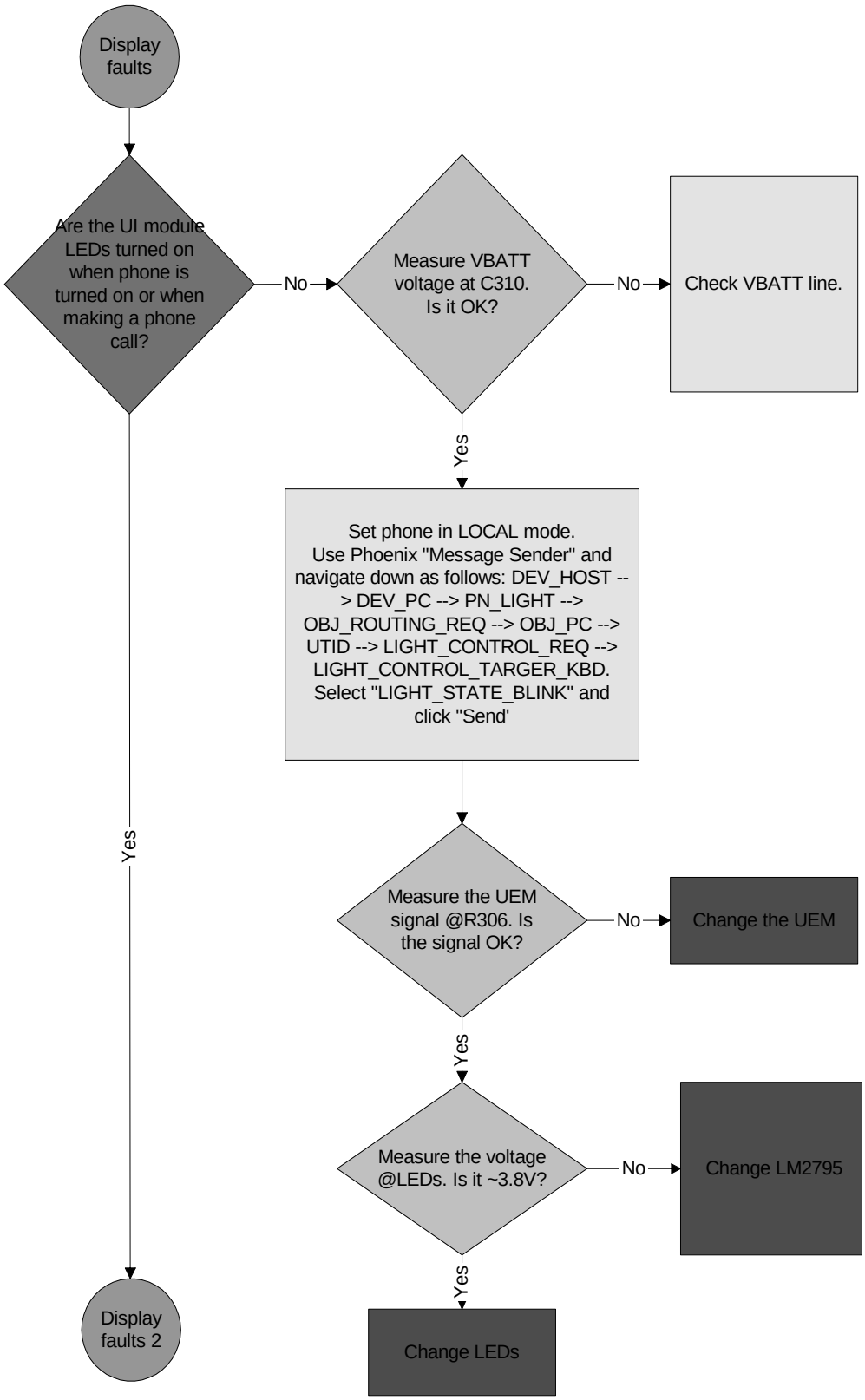

Audio faults
Is the earpiece working?
No
Change earpiece. Is it working now?
Yes
Retest
Yes
No
Set phone in LOCAL mode. Use Phoenix "Baseband Audio Control" and set the following: Enable Tx, Enable Rx, Select MIC2 (0dB), Enable earpiece and enable digital loop back only.
Inject a 1KHz sine signal 20mVp-p on XMIC (pin9/10 of the bottom connector
Is the signal coming out of the UEM on EARP and EARN?
No
Probe signal on R162, R155, V152, C154, C155, R152, R150, C151, C153, L120, R180. Check the bias voltage on one end of C193 (2.1V). If OK, change UEM
Yes
Check R150, C180, and C181. If OK, then change earpiece.
Yes
Audio faults 2

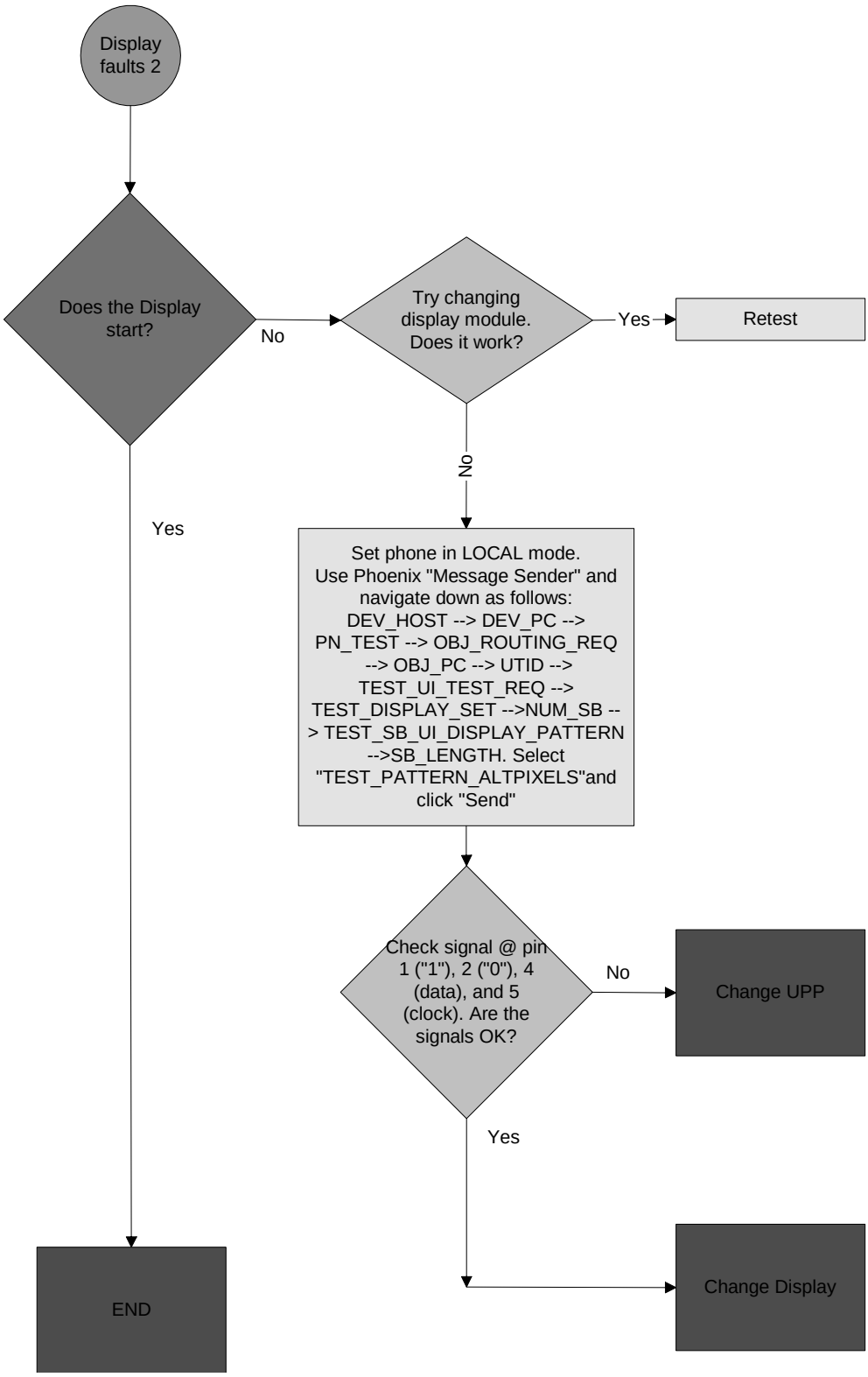

Audio faults 2
Is the microphone working?
No
Change the microphone. Is it working now?
Yes
Retest
No
Yes
Set phone in LOCAL mode. Use Phoenix "Baseband Audio Control" and set the following: Enable Tx, Enable Rx, Select MIC1, Enable HF only (differential ended). Talk through the microphone.
Measure MICB1 at C195. Is it ~2.1V?
No
Check C195, R176, R178. If OK, change UEM
Yes
Is the signal going to the UEM at MICP and MICN at L122 and C174?
No
If connection is OK at C175 and L122, then change microphone
Yes
Is the signal going out of the UEM at XEAR, pin 10 on the bottom connector?
No
Check if R160 is shorted to GND. If OK, change UEM
Yes
Retest
Audio faults 3


Audio faults 3
Is MIDI working?
No
Measure VBATT voltage from C196. Is it OK?
No
Check VBATT line.
Yes
Yes
Set phone in LOCAL mode. Use Phoenix to digital loop MIC1 to HF single-ended output. Also, set GenIO(28) high.
Talk to MIC1. Check signal @C157. Is signal OK?
No
Change the UEM
Yes
Check signal @MIDI speaker pads. Is signal OK?
Yes
Change speaker
No
Change MIDI amplifier N150
Audio faults 4

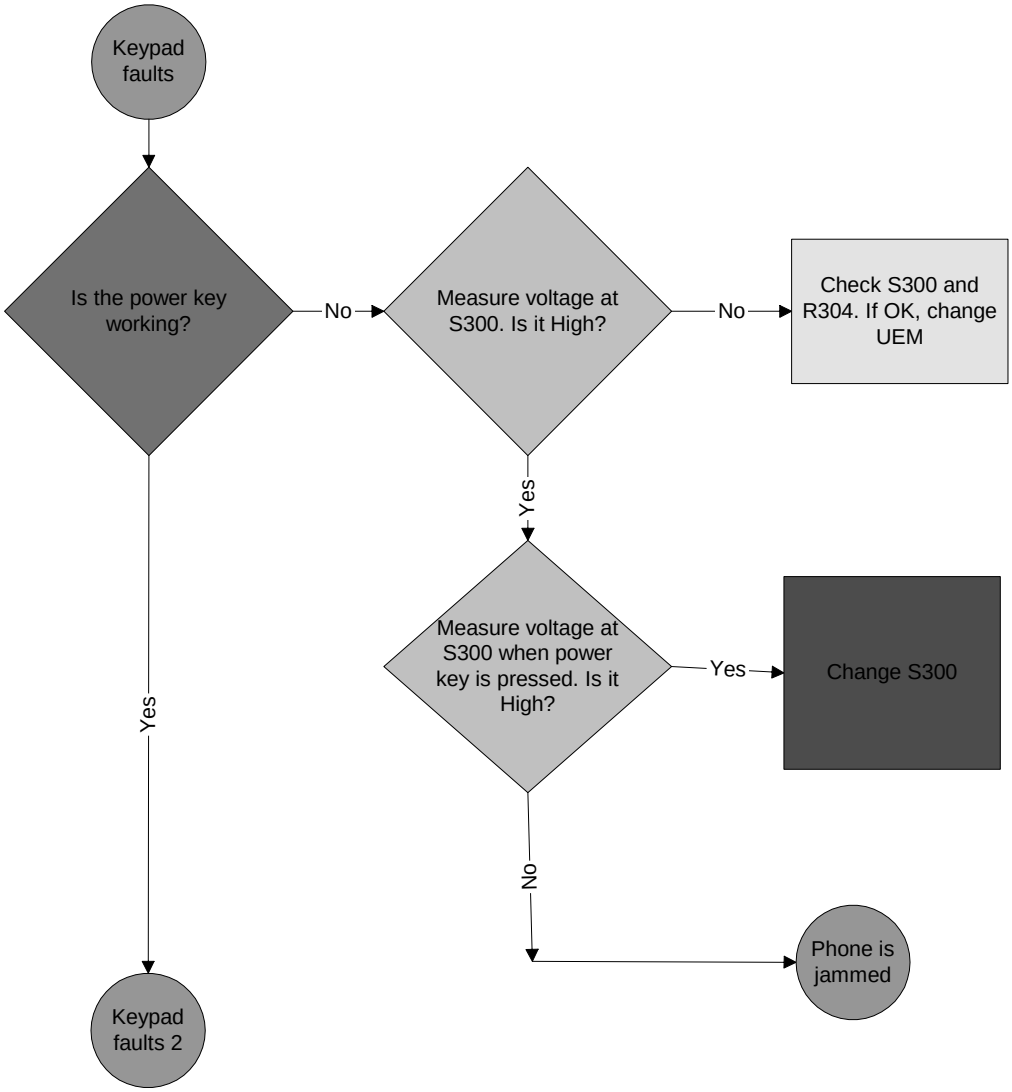

Audio faults 4
Is VIBRA working?
No
Measure VBATT voltage pin 1 of M300. Is it OK?
No
Check VBATT line.
Yes
Yes
Set phone in LOCAL mode. Use Phoenix "Message Sender" and navigate as follows: DEV_HOST --> DEV_PC --> PN_ACCESSORY --> PN_OBJ_ROUTING_REQ --> PN_OBJ_PC --> UTID_100 --> ACC_VIBRA_CTRL_REQ. Select "ACC_ON" and click "Send'
Measure the UEM signal on pin 2 of M300. Is the signal OK?
No
Change the UEM
Yes
Change VIBRA
END

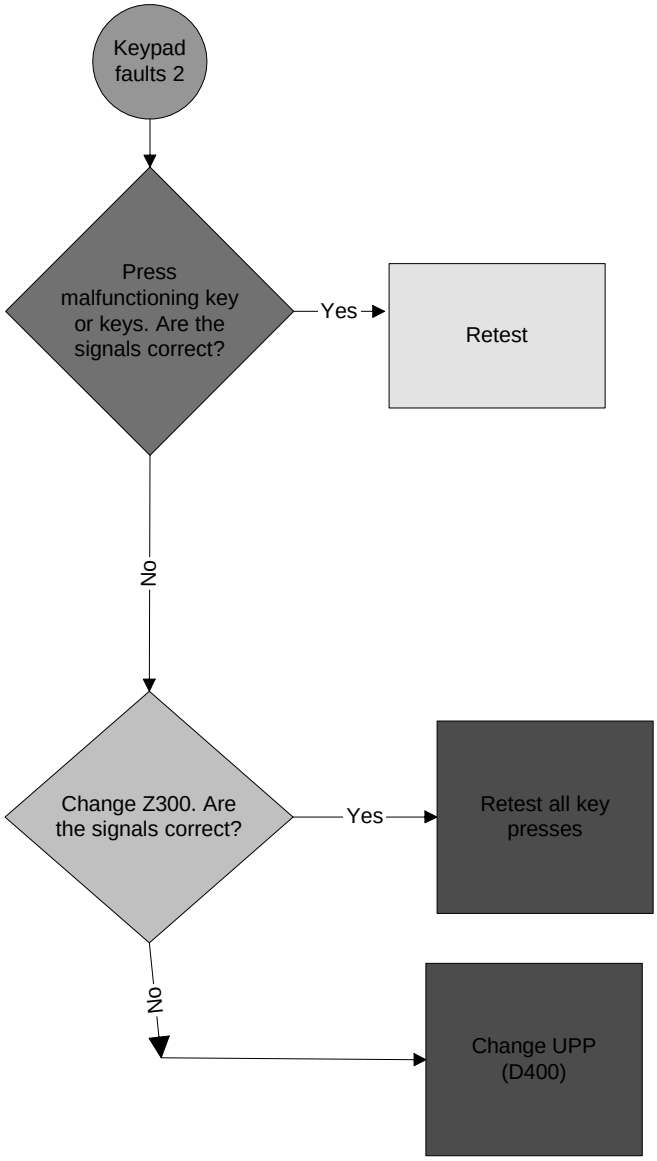
Display faults


Display faults
Are the UI module LEDs turned on when phone is turned on or when making a phone call?
No
Measure VBATT voltage at C310. Is it OK?
No
Check VBATT line.
Yes
Set phone in LOCAL mode. Use Phoenix "Message Sender" and navigate down as follows: DEV_HOST --> DEV_PC --> PN_LIGHT --> OBJ_ROUTING_REQ --> OBJ_PC --> UTID --> LIGHT_CONTROL_REQ --> LIGHT_CONTROL_TARGER_KBD. Select "LIGHT_STATE_BLINK" and click "Send'
Yes
Measure the UEM signal @R306. Is the signal OK?
No
Change the UEM
Yes
Measure the voltage @LEDs. Is it ~3.8V?
No
Change LM2795
Yes
Change LEDs
Display faults 2


Display faults 2
Does the Display start?
No
Try changing display module. Does it work?
Yes
Retest
No
Yes
Set phone in LOCAL mode. Use Phoenix "Message Sender" and navigate down as follows: DEV_HOST --> DEV_PC --> PN_TEST --> OBJ_ROUTING_REQ --> OBJ_PC --> UTID --> TEST_UI_TEST_REQ --> TEST_DISPLAY_SET -->NUM_SB --> TEST_SB_UI_DISPLAY_PATTERN -->SB_LENGTH. Select "TEST_PATTERN_ALTPIXELS"and click "Send"
Check signal @ pin 1 ("1"), 2 ("0"), 4 (data), and 5 (clock). Are the signals OK?
No
Change UPP
Yes
Change Display
END

Keypad faults




Keypad faults 2
Press malfunctioning key or keys. Are the signals correct?
Yes
Retest
No
Change Z300. Are the signals correct?
Yes
Retest all key presses
No
Change UPP (D400)